OPERATING AND SERVICE MANUAL

5005A
Signature Multimeter

SERIAL PREFIX: 2112

This manual applies to Serial Prefix 2112, unless accompanied by a Manual Change Sheet indicating otherwise.

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WARNING

THE SERVICE INFORMATION IS OFTEN USED WITH POWER SUPPLIED AND PROTECTIVE COVERS REMOVED FROM THE 5005A. ENERGY AVAILABLE AT MANY POINTS MAY, IF CONTACTED, RESULT IN PERSONAL INJURY.

WARNING

LINE VOLTAGE IS EXPOSED WITHIN THE 5005A EVEN WHEN THE LINE SWITCH IS SET TO OFF. REMOVAL OF THE POWER CORD IS NECESSARY TO FULLY UNPOWER THE 5005A.

WARNING

ALL TROUBLESHOOTING PROCEDURES REQUIRE INTERNAL ACCESS TO THE INSTRUMENT WITH THE PROTECTIVE COVERS REMOVED. THESE PROCEDURES SHOULD BE PERFORMED ONLY BY SERVICE-TRAINED PERSONNEL WHO ARE AWARE OF THE HAZARDS INVOLVED.

WARNING

BEFORE SWITCHING ON THIS INSTRUMENT, THE PROTECTIVE EARTH TERMINAL OF THIS INSTRUMENT MUST BE CONNECTED TO THE PROTECTIVE CONDUCTOR OF THE (MAINS) POWER CORD. THE MAINS PLUG SHALL ONLY BE INSERTED IN A SOCKET OUTLET PROVIDED WITH A PROTECTIVE EARTH CONTACT. THE PROTECTIVE ACTION MUST NOT BE NEGATED BY THE USE OF AN EXTENSION CORD (POWER CABLE) WITHOUT A PROTECTIVE EARTH (GROUNDING) CONDUCTOR.

WARNING

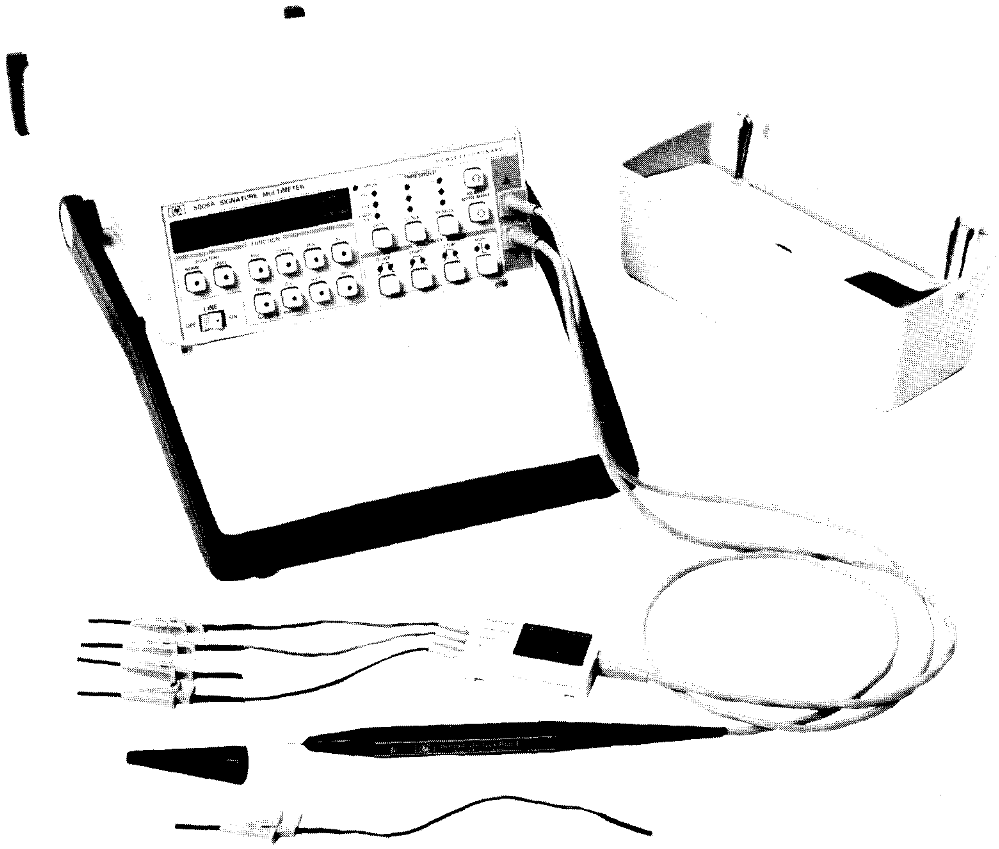
BEFORE THE INSTRUMENT IS SWITCHED ON, ALL PROTECTIVE EARTH TERMINALS, EXTENSION CORDS, AUTO TRANSFORMERS, AND DEVICES CONNECTED TO IT SHOULD BE CONNECTED TO A GROUNDED SOCKET. ANY INTERRUPTION OF THE PROTECTIVE EARTH GROUNDING WILL CAUSE A POTENTIAL SHOCK HAZARD THAT COULD RESULT IN PERSONAL INJURY.

WARNING

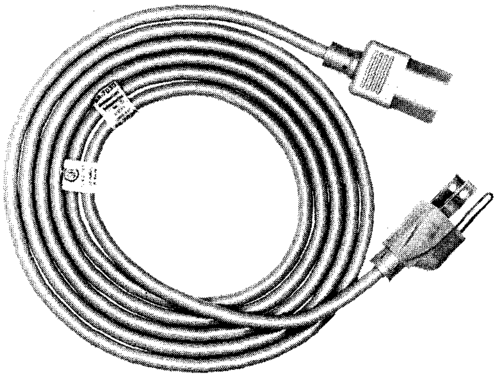
THE GROUND TEST LEADS ON THE POD AND DATA PROBE ARE TIED TO THE CHASSIS GROUND OF THE INSTRUMENT AND SHOULD NOT BE CONNECTED TO A VOLTAGE OTHER THAN GROUND FOR MEASUREMENTS.

WARNING

ONLY FUSES WITH THE REQUIRED RATED CURRENT AND SPECIFIED TYPE SHOULD BE USED. DO NOT USE REPAIRED FUSES OR SHORT-CIRCUITED FUSE-HOLDERS. TO DO SO COULD CAUSE A SHOCK OR FIRE HAZARD.



5005A SIGNATURE MULTIMETER AND EQUIPMENT SUPPLIED



**POWER CORD
PART NO. 8120-1378**

Figure 1-1. Model 5005A Signature Multimeter and Power Cable

SECTION I
GENERAL INFORMATION

1-1. INTRODUCTION

1-2. This Operating and Service Manual contains the information required to operate, test, adjust, and service the Hewlett-Packard Model 5005A Signature Multimeter. The multimeter with its supplied accessories is shown in *Figure 1-1*.

1-3. MANUAL SUMMARY

1-4. This manual is divided into eight sections, each covering a particular topic for the operation and service of the HP 5005A. The topics by section number are:

SECTION I, GENERAL INFORMATION. Provides the instrument specifications, instrument identification, accessories and recommended test equipment.

SECTION II, INSTALLATION. Provides information about initial inspection, preparation for use, storage and shipment.

SECTION III, OPERATION. Provides information about operating characteristics, panel features, Operator's Check, operating instructions, measurement procedures, and maintenance.

SECTION IV, PERFORMANCE TESTS. Provides abbreviated procedures for operational verification which give the operator a high degree of confidence that the 5005A is operating properly. Also provides expansive performance test procedures which test the electrical performance of the 5005A, using the specifications in *Table 1-1* as standards.

SECTION V, ADJUSTMENTS. Provides the procedures and adjustment locations required to properly maintain the instrument operating characteristics within specifications.

SECTION VI, REPLACEABLE PARTS. Provides ordering information for all replaceable parts and assemblies within the instrument.

SECTION VII, MANUAL CHANGES. This section is reserved for manual change information which effectively "backdates" the technical areas of the manual to apply to older instruments.

SECTION VIII, SERVICE. This section provides the instrument theory of operation, troubleshooting information, repair techniques, and schematic diagrams.

1-5. SPECIFICATIONS

1-6. The specifications for the 5005A are listed in *Table 1-1*. These specifications are the performance standards or limits against which the 5005A can be tested.

Table 1-1. 5005A Specifications

SIGNATURE

Display: 4 digits. Characters 0-9, ACFHPU.

Fault detection accuracy: 100% probability of detecting single-bit errors; 99.998% probability of detecting multiple-bit errors.

Minimum gate length: 1 clock cycle (1 data bit) between START and STOP.

Maximum gate length: no limit.

Minimum timing between gates: 1 clock cycle between STOP and START.

Data probe timing:

Setup time: 10 ns (data to be valid at least 10 ns before selected clock edge.)

Hold time: 0 ns (data to be held until occurrence of selected clock edge.)

START, STOP, QUAL timing:

Setup time: 20 ns (signals to be valid at least 20 ns before selected clock edge.)

Hold time: 0 ns (signals to be held until occurrence of selected clock edge.)

CLOCK timing:

Maximum clock frequency: 20 MHz.

Minimum pulse width: 15 ns in high or low state.

Supplemental characteristics

Front panel indicators: flashing GATE light indicates detection of valid START, STOP, CLOCK conditions. Flashing UNSTABLE light indicates a difference between 2 successive signatures, and possible intermittent faults. Edge select lights indicate active edges for START, STOP, CLOCK and QUAL inputs.

Qualify mode: allows clock data qualification by an external signal.

DATA probe input impedance: 50 kΩ to the average value of "0" and "1" threshold settings (±6V max); 10 pF.

START, STOP, CLOCK, QUAL input impedance: 100 kΩ; 10 pF.

FREQUENCY

Display: 5 digits.

Ranges: 100 kHz, 1 MHz, 10 MHz, 50 MHz, autoranged.

Resolution: 1 LSD (1 Hz on 100 kHz range).

Accuracy: ±0.01% of reading ±1 count.

Supplemental characteristics

Minimum pulse width: 10 ns in high or low state.

Gate time: 1 s, fixed.

Input impedance: 50 kΩ to the average value of "0" and "1" threshold settings (±6V max); 10 pF.

TOTALIZING

Display: 5 digits.

Range: 0-99,999 counts.

Resolution: 1 count.

Accuracy: ±1 count.

Supplemental characteristics

Maximum input frequency: 50 MHz, with a minimum pulse width of 10 ns, and minimum pulse separation of 10 ns.

Minimum START/STOP pulse width: 20 ns.

DATA input impedance: 50 kΩ to the average value of "0" and "1" threshold settings (±6V max); 10 pF.

START, STOP input impedance: 100 kΩ; 10 pF.

TIME INTERVAL

Display: 5 digits.

Ranges: 10 ms, 100 ms, 1 s, 10 s, 100 s, autoranged.

Resolution: 1 count (100 ns on 10 ms range).

Accuracy: ±0.01% of reading ±1 count.

Supplemental characteristics

Minimum START/STOP pulse width: 20 ns.

START, STOP input impedance: 100 kΩ; 10 pF.

RESISTANCE

Display: 4 or 5 digits, depending on range.

Ranges: 30 kΩ, 300 kΩ, 1 MΩ, 3 MΩ, 10 MΩ, autoranged.

Accuracy: (at 15°C-30°C).

RANGE	FULL SCALE	ACCURACY	DISPLAY RESOLUTION
30 kΩ	29.999 kΩ	±1% of reading ±2 Ω	1 Ω
300 kΩ	299.99 kΩ	±1% of reading	10 Ω
1 MΩ	999.9 kΩ	±1% of reading	100 Ω
3 MΩ	2999. kΩ	±10% of reading	1 kΩ
10 MΩ	10000. kΩ	±10% of reading	10 kΩ

Supplemental characteristics

Input impedance: 20 kΩ to +2V.

Resolution: Actual measurement resolution, at higher values of resistance (>10 kΩ), is a multiple of the display resolution listed above, but is always well within the specified accuracy.

Table 1-1. 5005A Specifications (Continued)

DC VOLTAGE

Display: 4½ digits.
Ranges: ±25V, ±250V, autoranged; referenced to earth ground.
Accuracy: (at 15°C-30°C).

RANGE	ACCURACY	RESOLUTION
25V	±0.1 % of reading ± 2mV	1mV
250V (<100V)	±0.25% of reading ±20mV	10mV
250V (≥100V)	±0.25% of reading ±20mV	100mV

Supplemental characteristics
Input impedance: 10 MΩ

DIFFERENTIAL VOLTAGE

Reading: Reads input voltage present at the probe and displays difference between it and voltage at the time ΔV key was depressed.
Specifications: Same as for DCV, above. Voltage range is determined by larger of 2 compared voltages. Accuracy is valid for 1 minute after ΔV key depression.

Supplemental characteristics
Same as for DCV, above.

PEAK VOLTAGE

Display: 3½ digits.
Range: 0 - ±12Vp.
Resolution: 50mV.
Accuracy: ±2% of reading ±5% of p-p signal ±100mV.

Supplemental characteristics
Minimum peak duration: 10 ns.
Maximum time between peaks: 50 ms.
Input impedance: 100 kΩ; 10 pF.

LOGIC THRESHOLDS

Preset thresholds: (All levels ±0.2V).

FAMILY	DATA "1"	DATA "0"	CLOCK-ST-SP-QL
TTL	2.0V	0.8V	1.4V
ECL	-1.1V	-1.5V	-1.3V
CMOS	3.5V	1.5V	2.5V

Adjustable thresholds: Each preset threshold can be adjusted.
Range: ±12.5V, in 50mV steps.
Accuracy: ±2% of setting, ±.2V.

Operating characteristics
Logic threshold circuitry is operative during NORM, QUAL, kHz, TOTLZ and ms measurements.

GENERAL

Data probe tip: Acts as high-speed logic probe in the NORM, QUAL, kHz and TOTLZ modes. Lamp indicates high, low, bad-level and pulsing states. Minimum detected pulse width is 10 ns.
Data probe protection:
Continuous overload:
DCV, ΔV, kΩ modes only: ±250V AC/DC.
All other modes: ±150V AC/DC, 20V rms at input frequencies > 2 MHz.
Intermittent overload: ±250V AC/DC, up to 1 min, for all modes.
Timing pod protection:
Continuous overload: ±100V AC/DC, 20V rms at input frequencies > 2 MHz.
Intermittent overload: ±140V AC/DC, up to 1 min.
Auxiliary power supply: Three rear-panel connectors supply 5V at 0.7A total for pulser, current tracer or microprocessor exerciser.
Operating temperature: 0°C to +55°C.
Operating humidity: 95% RH at +40°C, except as specified otherwise for DCV, ΔV and kΩ modes.
Power: Selectable 100V, 120V, 220V or 240V AC line (+5%-10%), 48-440 Hz. 35 VA maximum.
Weight: Net: 3.5 kg, 8.0 lbs. Shipping: 10 kg, 22.5 lbs.
Size: 90 mm high × 215 mm wide × 410 mm deep (3½ in × 8½ in × 16 in), excluding handle.

***Specifications** describe the instrument's warranted performance. *Supplemental characteristics* (shown in italics) are intended to provide information useful in applying the instrument, but are non-warranted performance parameters.

1-7. DESCRIPTION

1-8. The 5005A Signature Multimeter is a multipurpose instrument for troubleshooting electronic logic circuits to the component level. The 5005A can display digital "signatures" of logic circuits. This method of troubleshooting is called "signature analysis". Typically a logic product designed for signature analysis troubleshooting will have a programmed controller and a stored or externally-provided test program which can exercise most of the unit.

1-9. The 5005A also measures frequency, pulse counts, time intervals, DC voltages, voltage differences, positive or negative peak voltages, and resistances.

1-10. ACCESSORIES SUPPLIED

1-11. The accessories supplied with the 5005A are shown in *Figure 1-1.* Their description and part number are given below:

a. Depending on the customer's country, the line power cable supplied has one of six appropriate line (mains) connectors. Refer to *Figure 2-2,* Power Cable HP Part Numbers Versus Mains Plugs Available, for the part number of the correct cable.

b. Five detachable "grabber" test connectors are supplied with the 5005A. Their part number is 10230-62101. Refer to Section III for a description and use.

c. One ground lead for the data probe is supplied with the 5005A. Its part number is 05005-60116. One data probe tip cover is supplied. Its part number is 00547-40005.

1-12. INSTRUMENT AND MANUAL IDENTIFICATION

1-13. The instrument serial number is located just below the power input module on the rear panel. The serial number is in the form: 0000A00000. It is in two parts; the first four digits and the letter are the serial prefix and the last five digits are the suffix. The prefix is the same for all identical instruments; it changes only when a change is made to the instrument. The suffix however, is assigned sequentially and is different for each instrument. The contents of this manual applies to instruments with the serial number prefix(es) listed under SERIAL NUMBERS on the title page.

1-14. An instrument manufactured after the printing of this manual may have a serial number prefix that is not listed on the title page. This unlisted serial number prefix indicates the instrument is different from those described in this manual. The manual for this newer instrument is accompanied by a yellow Manual Changes supplement. This supplement contains "change information" that explains how to adapt the manual to the newer instrument.

1-15. In addition to change information, the supplement may contain information for correcting errors in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard.

1-16. For information concerning a serial number prefix that is not listed on the title page or in the Manual Changes supplement, contact your nearest Hewlett-Packard office.

NOTE

Two manuals describe the 5005A. The OPERATING MANUAL has only the first four sections. (Keep it with the 5005A.) The OPERATING AND SERVICE MANUAL has all eight sections. (Keep it in your calibration/repair department.)

1-17. SAFETY CONSIDERATIONS

1-18. The 5005A is a Safety Class 1 instrument provided with a protective earth terminal. Safety information pertinent to the operation and servicing of this instrument is included in appropriate sections of this manual.

1-19. Safety Symbols

NOTE

The symbol ⚠ (ATTENTION), which appears on the instrument, indicates the user should refer to the instruction manual before operating, to avoid possible damage to the instrument.

1-20. The following safety symbols are used on equipment and in manuals:

⚠	Instruction manual symbol. The product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the instrument.
ϟ	Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts must be so marked).
⏚ OR (⏚)	Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.
(⏚)	Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. A terminal marked with the symbol must be connected to ground in the manner described in the installation (operating) manual, and before operating the equipment.
⫫ OR ⊥	Frame and chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.
∿	Alternating current (power line).
⎓	Direct current (power line).
≂	Alternating or direct current (power line).
WARNING	The WARNING signal denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury.
CAUTION	The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

1-21. RECOMMENDED TEST EQUIPMENT

1-22. Equipment required to maintain the HP Model 5005A is listed in *Table 1-2*. Other equipment can be substituted if it meets or exceeds the critical specifications listed in the table.

Table 1-2. Recommended Test Equipment

Equipment	Required Characteristics	Used For				Recommended HP Model
		Adjustments	Op. Verification	Performance Tests	Troubleshooting	
Sig. Multimeter	See *Table 1-1*				X	5005A
Digital Voltmeter	+.001% acc.	X		X	X	3455A
2 Pulse Generators	50MHz Rate <5ns transition time			X		8012A
Pulse Generator	Presettable single-shot bursts			X		8011A/W OPT 001
Universal Counter	100MHz+TI 1ns Resolution			X		5370A
Universal Counter	100MHz			X		5316A
Pulse Generator	100MHz Rate <2ns transition time	X				8007B
Power Supply	±300VDC			X		6209B
Power Supply	0-30 VDC, ADJ 10MV Resolution			X		6216A
Oscilloscope	100MHz BW	X			X	1740A
Oscilloscope	275MHz BW			X		1725A
Function Generator	0.1Hz to 1MHz		X			3312A
Function Generator	50MHz			X		8165A
Logic Lab Breadboard				X		5035T
Microprocessor Lab			X*			5036A
Probe Set					X	5022A
Tuning Wand	Ceramic Wand	X				8710-0033

*Any instrument with an HP compatible digital signature analysis capability can be substituted here.

SECTION II
INSTALLATION

2-1. INTRODUCTION

2-2. This section contains information for unpacking, inspection, installation and storage.

2-3. UNPACKING AND INSPECTION

2-4. If the shipping carton is damaged, inspect the instrument for visible damage (scratches, dents, etc.). If the instrument is damaged, notify the carrier and the nearest Hewlett-Packard Sales and Service Office immediately (offices are listed at the back of this manual). Keep the shipping carton and packing material for the carrier's inspection. The Hewlett-Packard Sales and Service Office will arrange for repair or replacement of your instrument without waiting for the claim against the carrier to be settled.

2-5. PREPARATION FOR USE

CAUTION

Before connecting the instrument to ac power lines, be sure that the voltage selector is properly positioned as described below.

2-6. Power Requirements

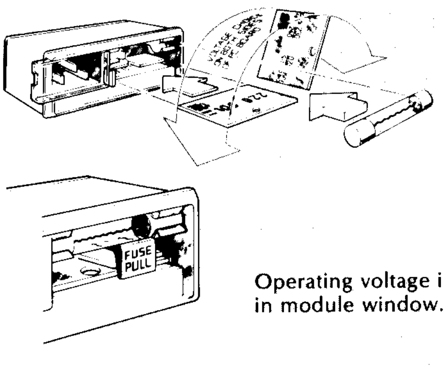
2-7. The 5005A requires an ac line power source of 100V, 120V, 220V, or 240V, +5% -10%, 48 to 440 Hz single phase. Power consumption is 35 VA maximum.

2-8. Line Power Module

2-9. The 5005A is provided with a line power module, which contains the main line fuse and a removable printed-circuit board. The printed-circuit board is installed in the line module in one-of-four positions, to select 100, 120, 220, or 240 Vac operation. Before applying power, verify that the printed-circuit board voltage selector is properly positioned for the desired ac supply voltage, and that the correct fuse is installed.

SELECTION OF OPERATING VOLTAGE

1. Open cover door and rotate fuse-pull to left.
2. Select operating voltage by orienting PC board to position desired voltage on top-left side. Push board firmly into module slot.
3. Rotate fuse-pull back into normal position and re-insert fuse in holders, using caution to select correct fuse value (.25A Slow Blow, 250V for 220 and 240V and 0.5A Slow Blow, 250V for 100 and 120V).



Operating voltage is shown in module window.

Figure 2-1. Line Voltage Selection

2-10. Selection of Operating Voltage and Main Line Fuse

2-11. Power line connections are selected by the position of the plug-in printed circuit board in the line power module. When the PC board is inserted into the module, the visible markings on the board indicate the configured line voltage. When converting from one line voltage to another, the power cord must be disconnected from the power module to allow the sliding window to be moved, which exposes the fuse and PC board compartment. To replace the main power fuse or change the selected line voltage, perform the following steps. Also see *Figure 2-1.*

1. Remove the power cord, and slide the fuse compartment window to the left.
2. Gently pull the FUSE PULL tab out and to the left. This frees one end of the fuse for easier removal, and allows access to the PC voltage selector board.
3. Select the operating voltage by orienting the PC board such that the desired voltage label appears on the top side and left half of the board. Push the board firmly into the PC board slot, located below the fuse. When fully seated, the configured operating voltage will be the only visible label.
4. Rotate the FUSE PULL tab back to its normal position. Insert the fuse by positioning against the snap-in connectors, and pressing in both ends. Be sure to install the correct fuse value; 0.5A/250V Slow Blow for 100V & 120V operation or .25A/250V Slow Blow for 220V & 240V operation.

2-12. Power Cable

2-13. The 5005A is shipped with a three-wire power cable. When the cable is connected to an appropriate ac power source, this cable connects the instrument chassis to earth ground. The type of power cable plug shipped with each instrument depends on the country of destination. Refer to *Figure 2-2* for the part numbers of the power cable and plug configurations available.

WARNING

BEFORE SWITCHING ON THIS INSTRUMENT, THE PROTECTIVE EARTH TERMINAL OF THIS INSTRUMENT MUST BE CONNECTED TO THE PROTECTIVE CONDUCTOR OF THE (MAINS) POWER CORD. THE MAINS PLUG SHALL ONLY BE INSERTED IN A SOCKET OUTLET PROVIDED WITH A PROTECTIVE EARTH CONTACT. THE PROTECTIVE ACTION MUST NOT BE NEGATED BY THE USE OF AN EXTENSION CORD (POWER CABLE) WITHOUT A PROTECTIVE EARTH (GROUNDING) CONDUCTOR.

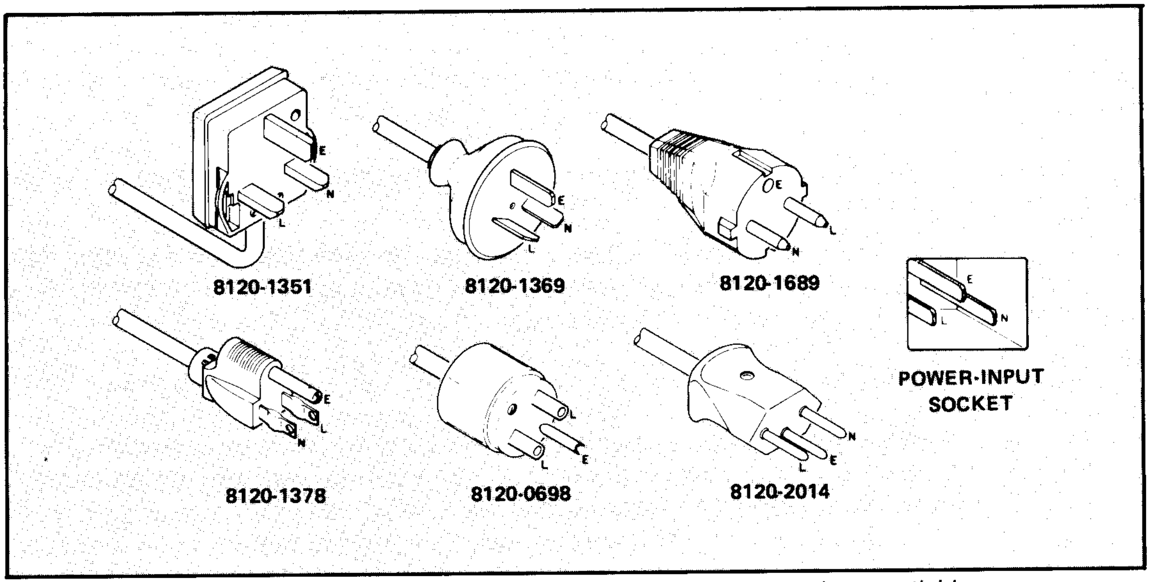


Figure 2-2. Power Cable HP Part Numbers versus Mains Plugs Available

2-14. Operating Environment

2-15. TEMPERATURE. The 5005A may be operated in temperatures from 0°C to +55°C.

2-16. HUMIDITY. The 5005A may typically be operated in environments with humidity up to 95% at 40°C. However, it should be protected from extreme temperatures which cause condensation in the instrument.

2-17. ALTITUDE. The 5005A may be typically operated at altitudes up to 4,600 metres (15,000 feet).

CAUTION

Before connecting the instrument to ac power lines, be sure that the voltage selector is properly positioned as described below.

2-18. STORAGE AND SHIPMENT

2-19. Environment

2-20. The instrument may be stored or shipped in environments within the following limits:

TEMPERATURE	-40°C to +75°C
HUMIDITY	Up to 95% noncondensing
ALTITUDE	7,620 metres (25,000 feet)

2-21. The instrument should also be protected from temperature and humidity extremes which cause condensation within the instrument.

2-22. Packaging

2-23. ORIGINAL PACKAGING. Containers and materials identical to those used in factory packaging are available through Hewlett-Packard offices. If the instrument is being returned to

Hewlett-Packard for servicing, attach a tag indicating the type of service required, return address, model number, and full serial number. Also, mark the container FRAGILE to ensure careful handling. In any correspondence, refer to the instrument by model number and full serial number.

2-24. OTHER PACKAGING. The following general instructions should be used for repacking with commercially available materials:

a. Wrap instrument in heavy paper or plastic. (If shipping to Hewlett-Packard office or service center, attach tag indicating type of service required, return address, model number, and full serial number.)

b. Use strong shipping container. A double-wall carton made of 350-pound test material is adequate.

c. Use a layer of shock-absorbing material 70 to 100 mm (3- to 4-inch) thick around all sides of the instrument to provide firm cushioning and prevent movement inside container. Protect control panel with cardboard.

d. Seal shipping container securely.

e. Mark shipping container FRAGILE to ensure careful handling.

f. In any correspondence, refer to instrument by model number and full serial number.

SECTION III
OPERATION

3-1. INTRODUCTION

3-2. This section gives complete operating information for the 5005A Signature Multimeter. Descriptions of all front panel controls, connectors, and indicators as well as an operator's check, operating instructions, and operator's maintenance are given.

3-3. The 5005A performs the analog measurements; DC volts (DCV), difference volts (ΔV), positive peak volts (Vp+), negative peak volts (Vp–), and resistance (kΩ), and digital measurements; Signature Analysis (NORM or QUAL), frequency (kHz), totalize (TOTLZ), and time interval (ms). In all digital measurements, selectable logic thresholds define the logic states for the incoming signals. All the measurements except Signature Analysis (NORM, QUAL) are standard measurements and require little explanation. However, Signature Analysis is a new concept and therefore is described in paragraph 3-16.

3-4. FRONT PANEL STORAGE COVER AND CABLE STORAGE

3-5. *Figure 3-1* shows the front panel storage cover with the handle locked in place for carrying. The line power cable is stored on the rear of the 5005A.

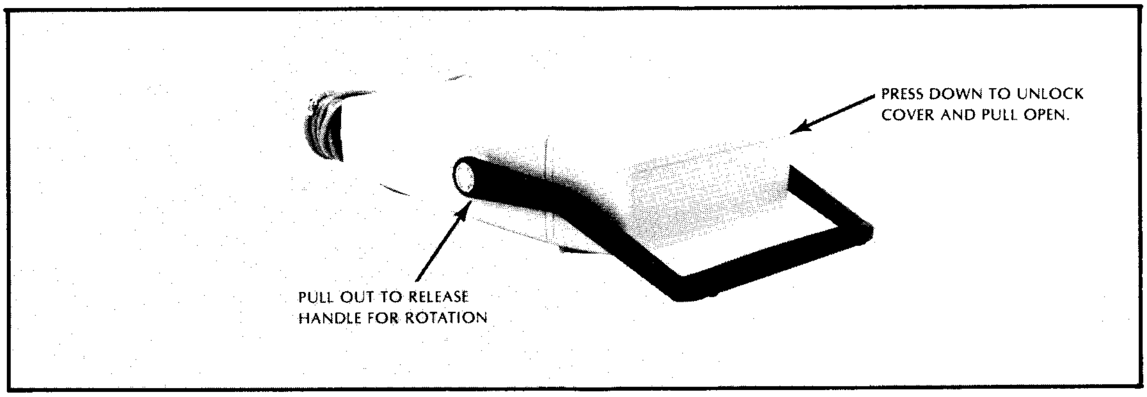


Figure 3-1. Storage Cover and Cable Storage

3-6. FRONT PANEL STORAGE COVER OPENING PROCEDURE

3-7. To open the front panel storage cover, perform the following procedures.

1. Pull gently at both side handle pivot points simultaneously, to unlock and rotate it.
2. Press down to open the front panel storage cover, exposing the 5005A front panel and Data Probe and Pod storage area.

3-8. DATA PROBE AND POD STORAGE

3-9. *Figure 3-2* shows the removable front panel storage cover open with the Data Probe and Pod in the recommended storage positions. The front panel storage cover should be used to store these components when the 5005A is not in use or is being transported.

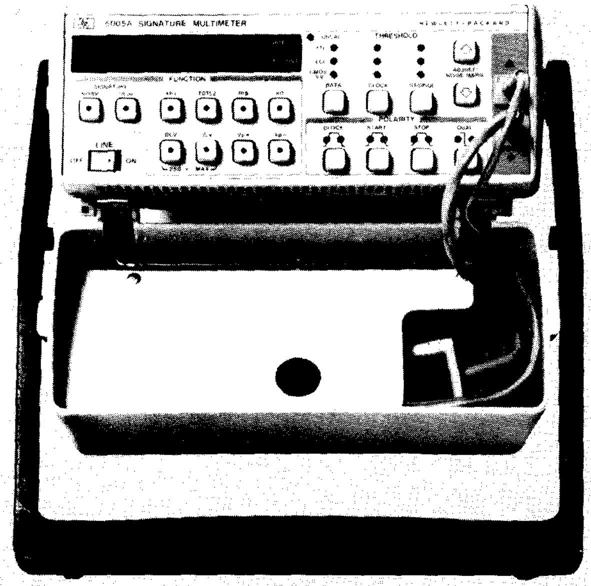

5005A SIGNATURE MULTIMETER
HEWLETT-PACKARD
THRESHOLD
FUNCTION
LINE
OFF
ON
DATA
CLOCK
STOP
POLARITY
START
QUAL

Figure 3-2. Data Probe and Pod Storage

3-10. FRONT PANEL STORAGE COVER REMOVAL PROCEDURE

3-11. To remove the front panel storage cover, perform the following procedures. Refer to *Figure 3-3*.

1. Unhook inside partition from front panel cover and raise the partition up.
2. Press in at one of the sides of the wire hinge-pin and remove inside partition.
3. Remove front panel storage cover.
4. To replace the cover and partition, perform the reverse of the removal procedure.

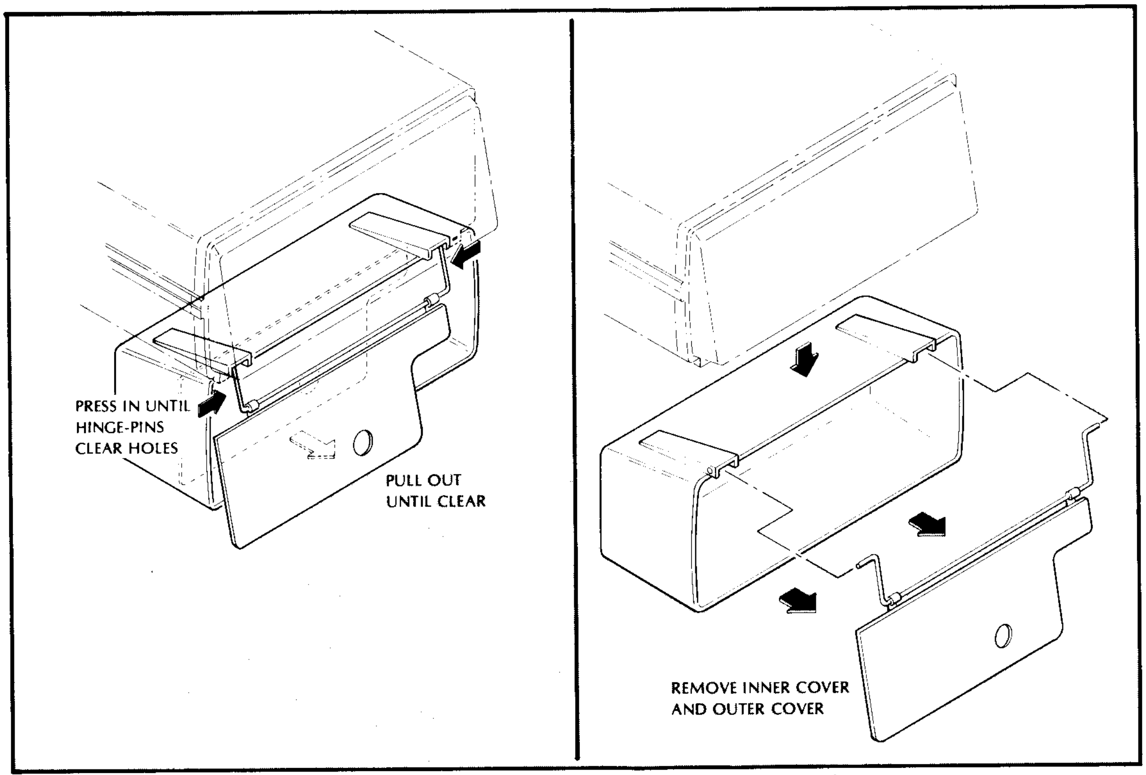

PRESS IN UNTIL HINGE-PINS CLEAR HOLES
PULL OUT UNTIL CLEAR
REMOVE INNER COVER AND OUTER COVER

Figure 3-3. Front Panel Storage Cover Removal

3-12. TYPICAL CONNECTIONS OF 5005A TO DEVICE UNDER TEST

3-13. *Figure 3-4* shows the 5005A Signature Multimeter connected to another device to take "signatures."

NOTE

The case of the 5005A is insulating plastic material so it will not cause electrical short circuits.

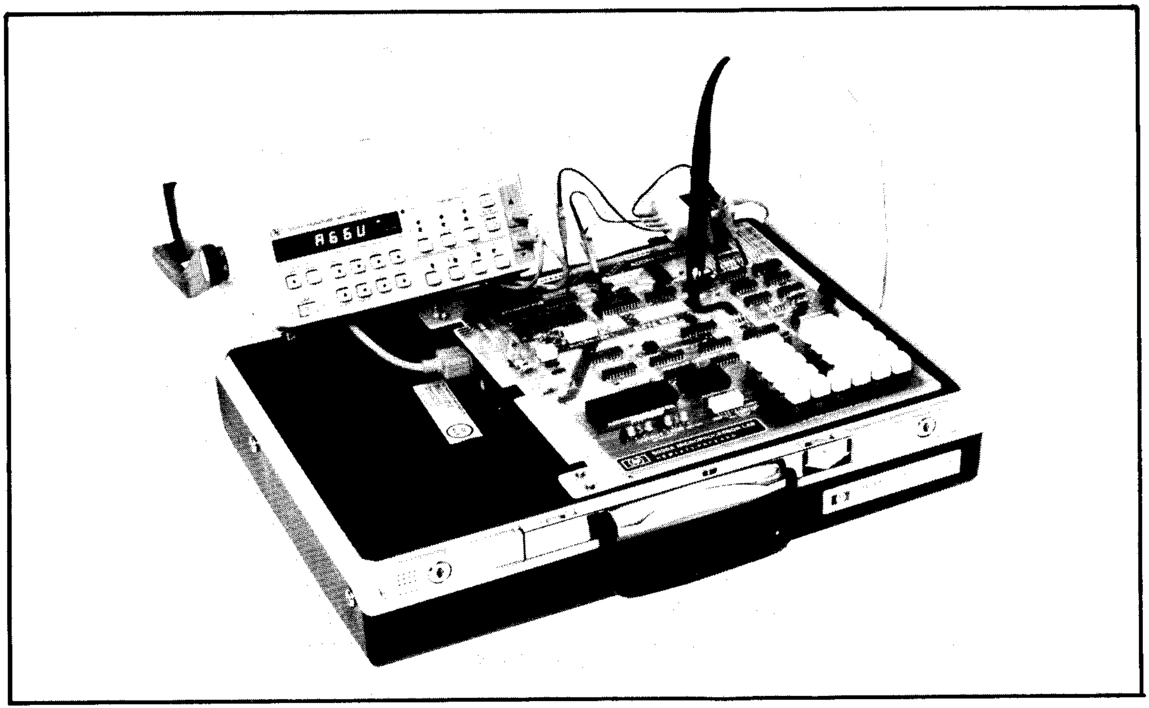


Figure 3-4. Typical Connections of 5005A to Device Under Test

3-14. TEST TERMINAL GRABBER CONNECTIONS

3-15. Five test-terminal grabber connectors are supplied with the 5005A. A grabber can be used on the end of the Timing Pod test leads to make reliable electrical connections from the 5005A to the instrument being tested. To connect a grabber to a test lead of the Pod, simply press the grabber on to the lead as shown in *Figure 3-5.* To place a grabber on the IC pin, grasp the grabber and compress the thumbhold. This allows the metal hook to open and be placed on the desired IC pin. To remove the grabber, compress the thumbhold and remove the grabber from the IC pin. The removable ground (⊥) test lead for the Data Probe also has a grabber.

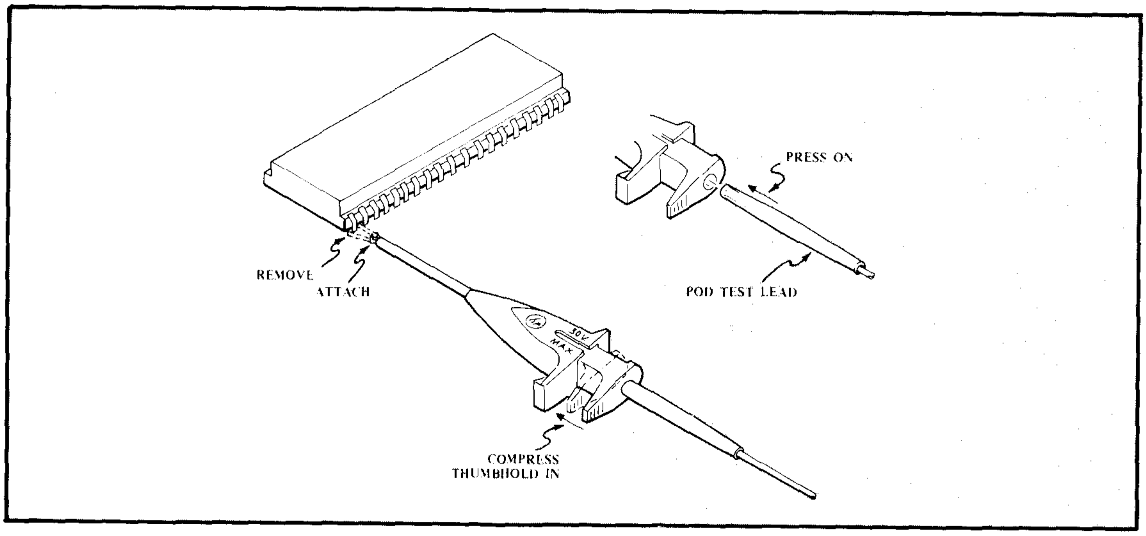
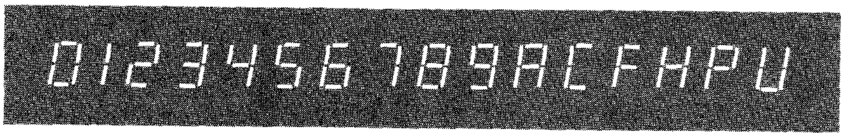


Figure 3-5. Test Terminal Grabber Connections

3-16. SIGNATURE ANALYSIS

3-17. The 5005A Signature Multimeter presents digital signatures with a four-character (symbol) display on its front panel. Each character, which can be any one of 16 symbols, is shown on a 7-segment light-emitting diode (LED) display. The 16 possible characters are:


0 1 2 3 4 5 6 7 8 9 A C F H P U

3-18. The characters presented on the display are special hexadecimal numbers which represent the residue in a CRC (Cyclical Redundancy Code) shift register in the 5005A after START and STOP signals have been received. The number of data bits between the START and STOP signals can be 1 to ∞ (infinity).

NOTE

No signature appearing on the 5005A display has any particular significance beyond being a correct (expected) signature or an incorrect signature. The number is, however, a residue in the 5005A converted to and displayed in special hexadecimal.

3-19. SIGNATURE ANALYSIS LITERATURE

3-20. Further Signature Analysis information literature is listed in *Application Note 222-0, An Index to Signature Analysis Publications.* This maintained document lists the description and part number of the available literature concerning digital Signature Analysis, which can be ordered through the nearest Hewlett-Packard Sales and Service Office.

3-21. HEXADECIMAL NUMBER SYSTEM SYMBOLS (DIGITS)

3-22. The four-character front panel Signature Analysis display presents numbers in a special set of hexadecimal symbols. The final six symbols are not the common hexadecimal symbols ABCDEF because the seven segment display of the 5005A cannot show a B or D that would be different from an 8 or 0 respectively (and several other symbols could be interpreted as another character when viewed upside-down e.g. E → 3). The actual characters are illustrated in paragraph 3-17.

3-23. PANEL FEATURES

3-24. Front and rear panel connectors, indicators, and controls of the 5005A are described in *Figures 3-8, 3-9, 3-10* and *3-11* respectively. These figures locate and describe all operator controls, connectors, and indicators.

3-25. OPERATOR'S CHECKS

3-26. A procedure to verify the basic operation of the 5005A is provided in *Table* 3-6. The check utilizes the instruments self-check cycle and verification of front panel indications. No additional equipment is required.

3-27. POWER-UP SELF CHECK

3-28. When the 5005A is turned-on, a power-up self-check cycle is automatically started. With no inputs applied, the sequence is as follows:

1. Initially, all segments, indicators, and pushbutton LEDs on the front panel and display are lighted except the GATE and UNSTABLE LED's which flash momentarily.
2. Then, after powering-up, the rising edge CLOCK ☐, START ☐, STOP ☐, the THRESHOLD TTL LED's, and the NORM ☐ pushbutton LED will light. The display will contain - - - -.

3-29. During this cycle, the microprocessor performs a check sum of the internal program in ROM and a bit pattern is written into and read from RAM. Additionally, a timer test, DVM test, internal count test, LED test, and a partial check of the D/A converter circuits are performed. A failure during the cycle will display a numbered error message, or will result in a visibly improper state of the front panel display and indicators. Refer to Error Messages, paragraph 3-34.

3-30. QUICK OPERATION TEST

3-31. The Quick Operation Test verifies other circuits not checked in the Power-Up Self-Check. The procedure is as follows:

1. Press the kΩ ⊡ pushbutton on the front panel. Verify that the display reads O P E N.

2. Connect Data Probe tip to the Timing Pod START/ST-SP (green), STOP/QUAL (red), and CLOCK (yellow) leads sequentially. Verify that the display reads approximately 100K ohms for each reading.
3. Connect Data Probe tip to the Timing Pod ground (black) lead. Verify that the display reads zero ohms.

3-32. CONDITIONAL DISPLAYS

3-33. Under certain circumstances the HP5005A will respond with a unique display, representative of a special condition. The possible conditional displays and the indicated meaning are listed in *Table 3-1* below.

Table 3-1. Conditional Displays

Function Mode	Display	Meaning
Signature Analysis NORM QUAL	- - - -	No measurement taken.
kHz	OFLO	Measurement overflow, input frequency ≥ 100 MHz.
TOTLZ	OFLO	Measurement overflow, events totalized > 99,999 counts.
ms	OFLO	Measurement overflow, time interval > 99,999 ms.
Vp+, Vp-	OL	Voltage peak ≥ 12.5 volts.
Vp+, Vp-	-OL	Voltage peak ≤ -12.5 volts.
⚠ DCV	OL -OL	Voltage ≥ 260 volts. Voltage ≤ -260 volts.
⚠ ΔV	OL -OL	Voltage of one reference point ≥ 260 volts. Voltage of one reference point ≤ -260 volts.
kΩ	OL -OL OL -OL OPEN	Drastic overload: ≈ 20 volts or greater. Positive source 2 volts connected. Negative source 2 volts connected. Open circuit.
All	ERRXX	Internal error with identifying number.

3-34. ERROR MESSAGES

3-35. Failures during the Power-Up Self-Test will result in a display of a numbered error message. There are 16 numbered Error Messages, as listed below. Refer to Section VIII in the Service Manual for additional information.

ERROR	MESSAGES
ERR00	ROM checksum error
ERR04	RAM read/write error
ERR06	Timer error
ERR07	DVM Zero offset measurement exceeds ±00200
ERR08	DVM data exceeds 32000
ERR09	DVM 10V calibration measurement exceeds 10.3V on 25V range
ERR10	DVM 10V calibration measurement is less than 9.3V on 25V range
ERR11	DVM 10V calibration measurement exceeds 10.3V on 250V range
ERR12	DVM 10V calibration measurement is less than 9.3V on 250V range

ERR13	Ohms 2V calibration exceeds 2.1V
ERR14	Ohms 2V calibration less than 1.9V
ERR15	Internal count test or keyboard error (illegal keycode)
ERR16	D/A converter Zero Offset exceeds 200 mV
ERR18	DVM measurement timeout — M/Z status incorrect
ERR19	DVM data transfer error-digit strobe status incorrect
ERR20	Keyboard encoder DATA VALID signal error

3-36. INSTRUMENTS COMPATIBLE WITH 5005A.

3-37. The 5005A is used to test the operation of electronic digital logic products with the signature analysis method.

3-38. OPERATING INSTRUCTIONS

WARNING

BEFORE THE INSTRUMENT IS SWITCHED ON, ALL PROTECTIVE EARTH TERMINALS, EXTENSION CORDS, AUTO TRANSFORMERS, AND DEVICES CONNECTED TO IT SHOULD BE CONNECTED TO A GROUNDED SOCKET. ANY INTERRUPTION OF THE PROTECTIVE EARTH GROUNDING WILL CAUSE A POTENTIAL SHOCK HAZARD THAT COULD RESULT IN PERSONAL INJURY.

WARNING

THE GROUND TEST LEADS ON THE POD AND DATA PROBE ARE TIED TO THE CHASSIS GROUND OF THE INSTRUMENT AND SHOULD NOT BE CONNECTED TO A VOLTAGE OTHER THAN GROUND FOR MEASUREMENTS.

WARNING

ONLY FUSES WITH THE REQUIRED RATED CURRENT AND SPECIFIED TYPE SHOULD BE USED. DO NOT USE REPAIRED FUSES OR CIRCUITED FUSE-HOLDERS. TO DO SO COULD CAUSE A SHOCK OR FIRE HAZARD.

CAUTION

Before the instrument is turned on, the Line Module must be set to match the voltage of the power line, or damage to the instrument could result.

3-39. The 5005A makes analog measurements; DCV, ΔV, Vp+, Vp–, kΩ, and digital measurements; NORM, QUAL kHz, TOTLZ, ms. In all digital modes, the 5005A interprets input signal levels according to the thresholds set. That is, the thresholds define the logic levels for the incoming signals.

3-40. General Set-Up Procedures

3-41. The general set-up procedures described below are to be used prior to performing the measurement set-ups in *Tables 3-7* through *3-15*.

1. Set the 5005A LINE switch to ON. The 5005A performs a power-up self-check and goes into NORM mode. (See paragraph 3-27.)
2. Select the desired FUNCTION pushbutton.
3. Select and set the THRESHOLD, if required.
4. Select and set the POLARITY edges or QUAL level, if required.
5. Connect the Timing Pod leads to the signals to be measured, if required.

3-42. Programming the Input Logic Levels

3-43. The 5005A is pre-programmed to trigger on standard logic thresholds. The 5005A automatically powers-up in the TTL logic family mode and triggers at the voltage values listed in *Table 3-2*. The logic family mode for DATA (Probe), CLOCK (Pod), and ST-SP-QL (Pod) can be changed by pressing the pushbutton corresponding to that input. To change from one logic family to another, press the appropriate threshold pushbutton (DATA, CLOCK, or ST-SP-QL) in rapid succession until the logic family (TTL, ECL, CMOS 5V) LED lights. The following examples describe this procedure.

1. Press the DATA ☐ pushbutton three times in succession. The first press displays the TTL High DATA THRESHOLD level (2.00H). The second press displays the TTL Low DATA THRESHOLD level (0.80L). The third press changes the DATA logic threshold levels to the next logic family (ECL) and displays the High DATA THRESHOLD level for that logic family (-1.10H). The programmed logic levels for the selected input (DATA, CLOCK, or ST-SP-QL) can be reviewed at any time by pressing the respective pushbutton once for the High level, and once more for the Low level. If no pushbuttons are pressed for approximately 2 seconds, the display will return to the previously set operating mode.
2. Press the CLOCK ☐ pushbutton two times in quick succession. The first press displays the CLOCK THRESHOLD TTL trigger level. The second press changes the CLOCK logic threshold level to the next logic family (ECL), and displays the new CLOCK THRESHOLD trigger level (-1.30).
3. Press the ST SP-QL ☐ pushbutton two times in quick succession. The first press displays the ST-SP-QL THRESHOLD TTL trigger level. The second press changes the ST-SP-QL logic threshold level to the next logic family (ECL) and displays the new ST-SP-QL THRESHOLD trigger level (-1.30).

Table 3-2. Logic Family Voltage Levels

	THRESHOLDS		
FUNCTION	**TTL**	**ECL**	**5V CMOS**
DATA	H 2.00V	-1.10V	3.50V
	L 0.80V	-1.50V	1.50V
CLOCK	1.40V	-1.30V	2.50V
ST-SP-QL	1.40V	-1.30V	2.50V

3-44. Threshold Level Setting and Adjustment

3-45. To change the value of a programmed threshold, within any logic family, the appropriate input threshold pushbutton (DATA, CLOCK, or ST-SP-QL) should be pressed until the level to be changed is displayed. An H or L will follow the displayed DATA THRESHOLD setting indicating the High or Low logic level currently set. To change the levels once the family (an H or L level for DATA) is selected, the ⇧ or ⇩ ADJUST/NOISE MARG pushbuttons are pressed, slewing the levels up or down respectively. The display will contain the current setting of the selected level. Setting and adjusting the input THRESHOLD levels is the same procedure for all measurement modes of the 5005A. For this reason, the following examples are given only for the NORM Signature Analysis mode. Refer to *Table 3-3* to indicate what THRESHOLD pushbuttons are active in each measurement mode.

1. To modify any of the input THRESHOLDs (High or Low DATA, CLOCK or ST-SP-QL) in any of the three logic families (TTL, ECL CMOS 5V, that THRESHOLD has to be displayed. This is done by pressing the corresponding THRESHOLD pushbutton, DATA, CLOCK, or ST-SP-QL until the required family LED is lighted and the threshold voltage is displayed; High or Low in case of DATA THRESHOLDS.
2. While the threshold voltage is displayed, it can be changed by pressing ⇧ or ⇩ ADJUST/NOISE MARG pushbuttons. A single depression will cause a 50mV step change, while holding the pushbutton down will cause a repeated stepping up or down with increasing speed. The maximum threshold voltage that can be set is ±12.5V. If no pushbuttons are pressed for approximately 2 seconds, the display will return to the previously set operating mode.
3. Whenever a threshold value, different from the preset (standard) value is displayed, the UNCAL (uncalibrated) LED will be lighted. The UNCAL LED will also be lighted in any measurement mode using one or more non-standard thresholds.

Table 3-3. Thresholds Used in Each Function

FUNCTION	**THRESHOLDS**		
	DATA	**CLOCK**	**ST-SP-QL**
NORM	*	*	*
QUAL	*	*	*
kHz	*		
TOTLZ	*		*
ms			*

*Indicates that particular THRESHOLD pushbutton is active.

3-46. Polarity Setting and Change

3-47. The procedure for setting and changing the POLARITY edges or level is contained in the following instructions. Refer to *Table 3-4* to indicate what POLARITY pushbuttons are active in each measurement mode.

1. To change the POLARITY edges (CLOCK, START, or STOP), the corresponding pushbutton CLOCK ☐, START ☐, or STOP ☐ is pressed and the desired edge-select LED is lighted.

2. To change the POLARITY level (QUAL), the corresponding pushbutton QUAL ● ● ☐ is pressed and the desired level LED is lighted. The left LED indicates High level active, and the right LED indicates Low level active.

Table 3-4. Polarities Used in Each Function

	POLARITY			
FUNCTION	**CLOCK**	**START**	**STOP**	**QUAL**
NORM	*	*	*	
QUAL	*	*	*	*
TOTLZ		*	*	
ms		*	*	

*Indicates that particular POLARITY pushbutton is active. POLARITY pushbuttons are active only in the four listed functions.

3-48. MEASUREMENT PROCEDURES

3-49. The following paragraphs describe the general measurement functions of the 5005A Signature Multimeter. *Tables 3-7* through *3-15* show general operating procedures with the 5005A in typical measurement setups.

3-50. Signature Analysis Measurements (NORM)

3-51. The 5005A can make Signature Analysis measurements on TTL, ECL, and 5V CMOS logic families. In addition, the threshold can be set to any level between -12.5V to +12.5V to make measurements on other logic families. The maximum input data rate is 20 MHz.

NOTE

> Each measurement function of the 5005A is selected by pressing its function pushbutton. If any threshold or polarity settings are relevant to this measurement, the corresponding LEDs will be lighted.

3-52. Signature Analysis Measurements (QUAL)

3-53. The 5005A Signature Analysis measurements can be enhanced with the Signature QUAL mode. The QUAL input, on the Timing Pod, is sensed by the 5005A as a Data Qualifier. Conceptually, the qualifier can be thought of as an "enable" signal. See *Figure* 3-6. The active qualified level (logic low or high) can be selected by the QUAL pushbutton. The START and STOP polarities can still be individually selected with the POLARITY pushbuttons. When in the QUAL Signature mode, the red Timing Pod lead becomes the QUAL (qualifier) input and the green timing Pod lead becomes the START **and** STOP input.

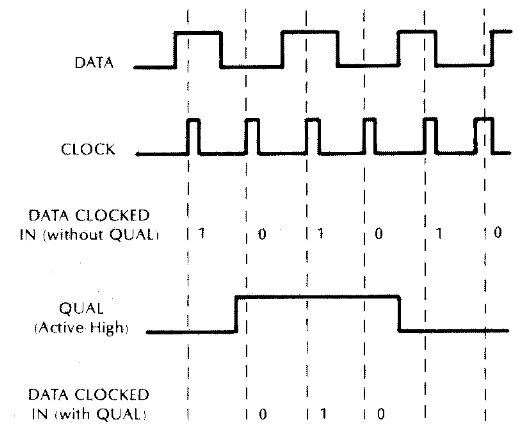

DATA
CLOCK
DATA CLOCKED
IN (without QUAL)
1
0
1
0
1
0
QUAL
(Active High)
DATA CLOCKED
IN (with QUAL)
0
1
0

Figure 3-6. Signature Analysis Measurements

3-54. Frequency Measurements

3-55. The 5005A makes frequency measurements, using TTL, ECL, and CMOS logic family thresholds, on input signals within the range of 0 to 50 MHz. These frequencies are counted directly with no prescaling techniques applied. The measurement gate time is fixed at one second. This gives a resolution of 1Hz up to 100kHz where the resolution becomes 1 LSD at a 5 digit display. The accuracy is ±0.01% of reading ±1 count.

3-56. Totalize Measurements

3-57. The 5005A can count the number of pulses occuring at the Data Probe between the START and STOP timing signals. In this mode, all the inputs (Start, Stop, and Data) are used asynchronously. The Clock input is not used. In the totalize mode, the 5005A can accumulate from 0 to 99,999 counts at a maximum rate of 50 MHz. *Figure 3-7* illustrates the timing relationship in the totalize measurement mode of operation.

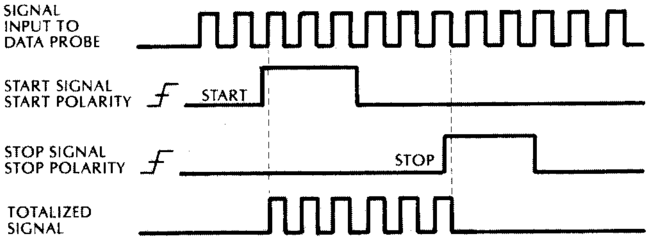

SIGNAL
INPUT TO
DATA PROBE
START SIGNAL
START POLARITY
START
STOP SIGNAL
STOP POLARITY
STOP
TOTALIZED
SIGNAL

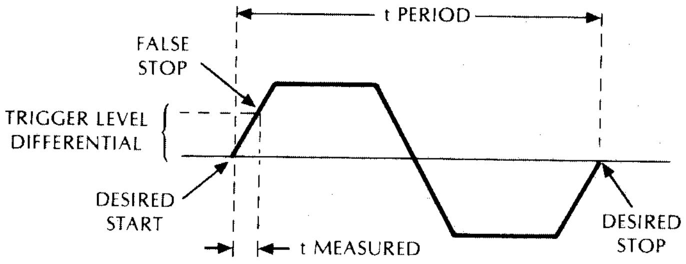
Figure 3-7. Totalize Measurement

3-58. Time Interval Measurements

3-59. Time interval measurements are made between a selected transition at the START lead and a consecutive transition on the STOP lead. The range is from 0 to 99,999 milliseconds with an accuracy of ±0.01% of reading ±1 count. Two source time interval measurements are displayed on a 5-digit display with a resolution of 100 ns.

NOTE

The Start and Stop trigger thresholds are connected together internally, but differences do exist in the trigger circuitry. This results in a small differential between the Start and Stop trigger levels. This condition allows the possibility of unexpected measurements during the Time Interval mode. For example:



For Time Interval measurements, the expected result would be the period (t period) of the input sinewave. However, depending on the trigger level differential, an unexpected measurement (t measured) may result.

3-60. Volts Peak, Plus or Minus Measurements

3-61. Peak voltages can be measured between ±12.0V provided the peak duration is ≥10ns and the rate is ≥20 Hz. The 3 1/2-digit display provides a resolution of 50mV with an accuracy of ±2% of reading ±5% of p-p signal ±100 mV.

⚠ 3-62. DC Volt Measurements

3-63. The 5005A can measure a maximum of ±250 VDC with a 10M input impedance and features auto ranging and auto polarity circuits. The 4 1/2-digit display gives a resolution of 1mV up to 25V, 10mV from 25V to 100V and 100mV from 100V to 250V. The accuracy is ±0.1% ±2mV up to 25V and ±0.25% ±20mV from 25V to 250V.

⚠ 3-64. Delta Volt Measurements

3-65. The 5005A can measure a difference in voltage levels up to ±250V (maximum differential 500V) with an input impedance of 10M. The 4 1/2-digit display gives a resolution of 1mV if both voltages are less than 25V, 10mV if the difference is from 25V to 100V, and 100mV if the difference is from 100V to 250V. The accuracy is ±0.1% ±2mV for both voltages less than 25V and ±0.25% otherwise. The "reference" for the difference measurement is determined from the voltage present at the probe (tip) at the time the ΔV function key is pressed. **In this mode, the Data Probe ground (if used) must be at earth potential.**

3-66. Resistance Measurements

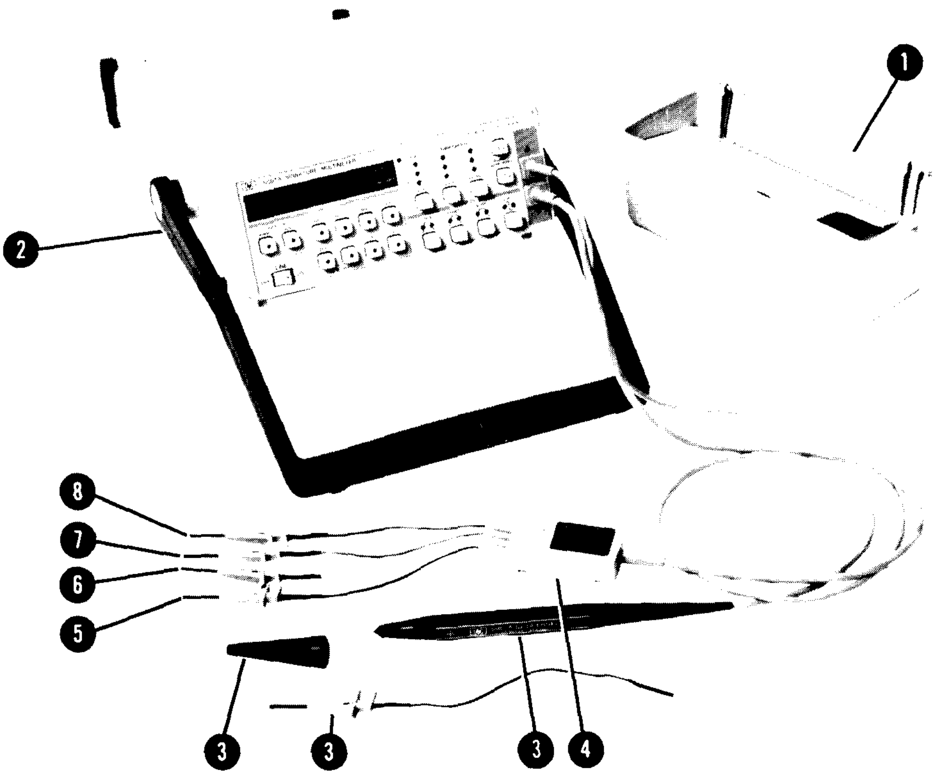
3-67. Resistance measurements can be made from 0 to 10MΩ. The resolution and accuracy are given in *Table 1-1*.

3-68. OPERATOR'S MAINTENANCE

3-69. The only maintenance the operator should normally perform is the replacement of the primary fuse on the 5005A. This fuse is located within the A7 Line Module Assembly. For instructions on how to change the fuse, refer to Section II, Line Voltage Selection.

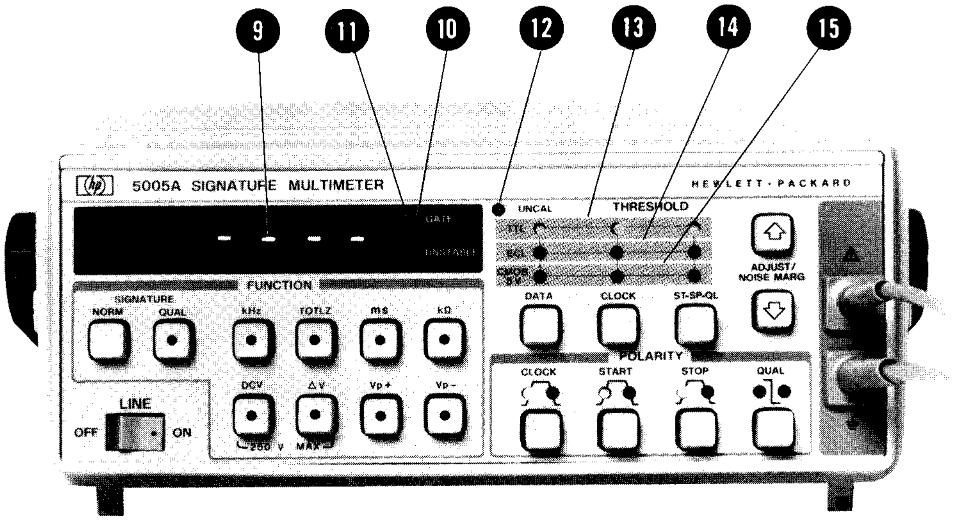
CAUTION

Make sure that only fuses with the required rated current and of the slow-blow type are used for replacement. The use of repaired fuses and the short-circuiting of fuse holders must be avoided.



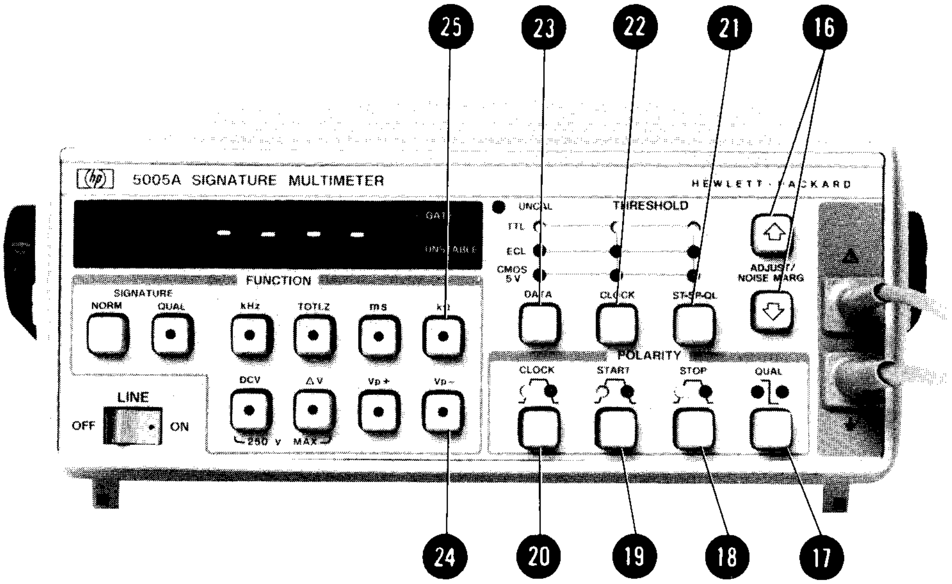
①	**STORAGE COVER**	Storage for the Data Probe, Timing Pod, and grabbers.
②	**HANDLE STAND**	The combination handle and stand can be rotated by gently pulling at both handle pivot points simultaneously and turning the handle to the desired position.
③	**DATA PROBE, PROTECTIVE COVER, and GND LEAD**	Point of entry for data from the unit being tested by the 5005A. The lamp above the probe tip indicates logic state of the data: On Bright=High, On Dim= Three-state, Off=Low. 10ns or greater pulses are stretched to 100ms. Note Probe ground connector (measuring earth terminal) and protective cap cover for Probe. Note that the probe acts as a logic probe in the SA, QUAL, KHz, and TOTLZ modes. The lamp has an undefined meaning in the DCV, VP+, VP–, ms, and ΔV modes.
④	**TIMING POD**	Four timing inputs, START/ST-SP, STOP/QUAL, CLOCK, and a common ground (⊥) are for connection to a Unit Under Test.
⑤	**GND POD LEAD**	Common (ground) lead (measuring earth terminal) for connection to Unit Under Test.
⑥	**CLOCK POD LEAD**	Point of entry for CLOCK signal from the Unit Under Test.
⑦	**STOP/QUAL POD LEAD**	Point of entry for STOP signal in NORM mode and QUAL signal in QUAL mode from the Unit Under Test.
⑧	**START/ST-SP POD LEAD**	Point of entry for START signal in NORM or QUAL mode and STOP and START signals in QUAL mode from the Unit Under Test.

Figure 3-8. Signature Multimeter, Probe and Pod Features


9
11
10
12
13
14
15
5005A SIGNATURE MULTIMETER
HEWLETT · PACKARD
GATE
UNSTABLE
UNCAL
THRESHOLD
TTL
ECL
CMOS 5V
ADJUST/ NOISE MARG
FUNCTION
SIGNATURE
NORM
QUAL
kHz
TOTLZ
ms
kΩ
DATA
CLOCK
ST-SP-QL
POLARITY
CLOCK
START
STOP
QUAL
LINE
OFF
ON
DCV
ΔV
Vp+
Vp−
250 V MAX

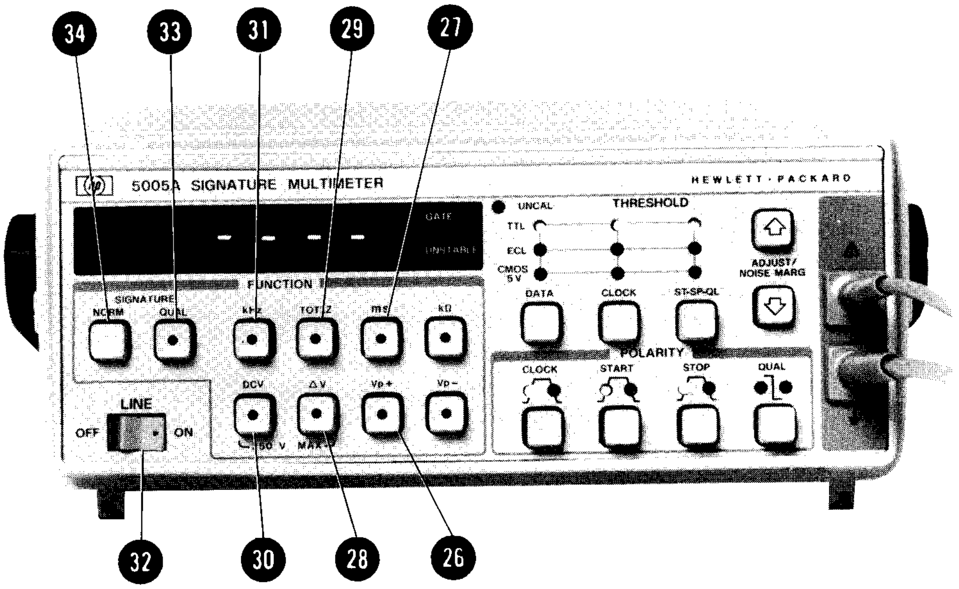
⑨	**DISPLAY**	Contains the five seven-segment LED displays, and the preceding minus sign.
⑩	**GATE LED**	Flashing of GATE LED indicates 5005A is being gated.
⑪	**UNSTABLE LED**	Indicates an unstable signature reading.
⑫	**UNCAL LED**	Indicates that one or more of currently used input threshold levels is adjusted to a non-standard value.
⑬	**TTL LEDs**	Indicates the respective thresholds are set to test TTL logic. The TTL LED will be lighted even if the thresholds have been modified by the user. The UNCAL LED will light to indicate this condition.
⑭	**ECL LEDs**	Indicates the respective thresholds are set to test ECL logic. The ECL LED will be lighted even if the thresholds have been modified by the user. The UNCAL LED will light to indicate this condition.
⑮	**CMOS LEDs 5V**	Indicates the respective thresholds are set to test 5V CMOS logic. The 5V CMOS LED will be lighted even if the thresholds have been modified by the user. The UNCAL LED will light to indicate this condition.

Figure 3-9. Front Panel Indicators


25
23
22
21
16
5005A SIGNATURE MULTIMETER
HEWLETT · PACKARD
UNCAL
THRESHOLD
TTL
ECL
CMOS 5 V
ADJUST/ NOISE MARG
FUNCTION
SIGNATURE
NORM
QUAL
kHz
TOTLZ
ms
kΩ
DATA
CLOCK
ST-SP-QL
POLARITY
CLOCK
START
STOP
QUAL
LINE
OFF
ON
DCV
ΔV
Vp+
Vp−
250 V MAX
24
20
19
18
17

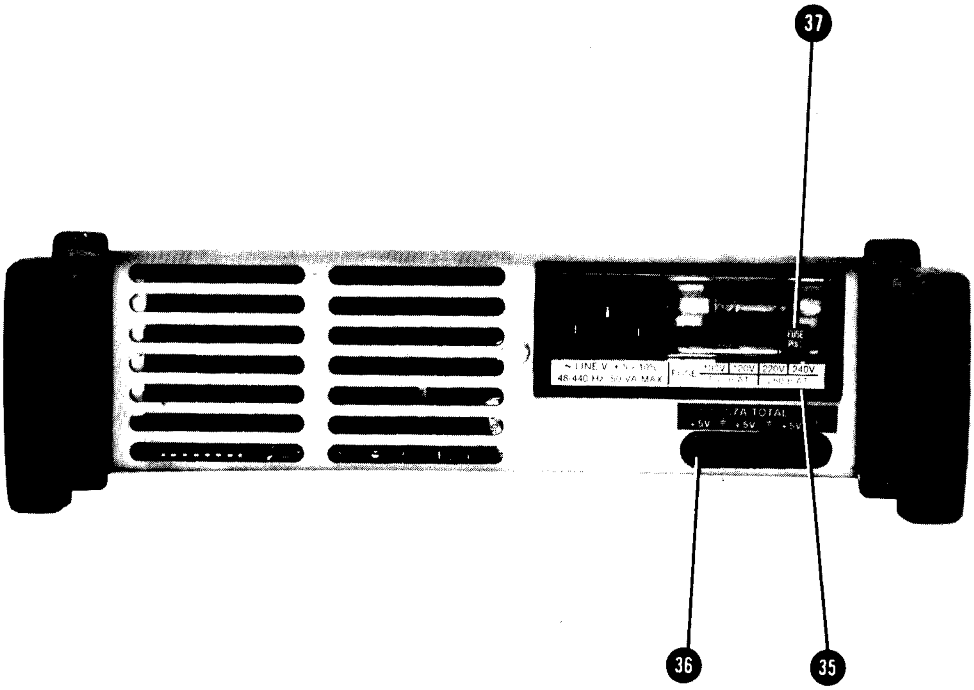
⑯	⇧ ADJUST/ NOISE MARG ⇩	Voltage threshold adjustment by single steps (or continuously if pressed-in and held) up or down in increments of 50 mV. Threshold adjustment pushbuttons can be used to check noise margins in the tested logic circuit.
⑰	**QUAL**	Selects whether the signature analysis is enabled by high or low level of the qualifying signal.
⑱	**STOP**	
⑲	**START**	These three pushbuttons select either the positive-going or negative-going transition of the input signals to be used for timing of the measurements.
⑳	**CLOCK**	
㉑	**ST-SP-QL (Start-Stop-Qual)**	This switch programs the ST-SP-QL inputs to operate with TTL, ECL, or 5V CMOS logic families.
㉒	**CLOCK**	This pushbutton programs the CLOCK input to operate with TTL, ECL, or 5V CMOS logic families.
㉓	**DATA**	This pushbutton programs the DATA input to operate with TTL, ECL, or 5V CMOS logic families.
㉔	**Vp−**	This pushbutton activates the negative peak voltage measurement.
㉕	**kΩ**	This pushbutton activates the resistance measurement. The measured resistance must be placed between the Data Probe tip and the Pod or Data Probe ground.

Figure 3-10. Front Panel Controls


34
33
31
29
27
5005A SIGNATURE MULTIMETER
HEWLETT · PACKARD
UNCAL
THRESHOLD
TTL
ECL
CMOS 5 V
ADJUST/ NOISE MARG
GATE
UNSTABLE
FUNCTION
SIGNATURE
NORM
QUAL
kHz
TOTLZ
ms
kΩ
DATA
CLOCK
ST-SP-QL
POLARITY
CLOCK
START
STOP
QUAL
DCV
ΔV
Vp+
Vp−
LINE
OFF
ON
50 V MAX
32
30
28
26

㉖	**Vp+**	This pushbutton activates the positive peak voltage measurement.
㉗	**ms**	The ms pushbutton activates the time interval measurements between the START and STOP signals at the Timing Pod leads.
㉘	**ΔV**	The delta volt pushbutton activates the 5005A to measure voltage levels at the Data Probe referenced to the voltage at the Data Probe at the time the ΔV pushbutton was pressed.
㉙	**TOTLZ**	This pushbutton activates the 5005A for counting the number of pulses at the input to the Data Probe occurring between the START and STOP pulses at the input to the Timing Pod.
㉚	**DCV**	The DCV pushbutton activates the 5005A to measure the voltage at the Data Probe tip referenced to ground.
㉛	**kHz**	The kHz pushbutton activates the 5005A for frequency measurements.
㉜	**LINE ON-OFF**	This is the main line switch for power to the 5005A.
㉝	**QUAL**	The QUAL pushbutton activates the 5005A for signature analysis in the qualified mode. The CLOCK, START, STOP edges, and QUAL level as well as the logic thresholds are programmable in this mode.
㉞	**NORM**	The NORM pushbutton activates the 5005A for signature analysis in the normal mode. The CLOCK, START, and STOP trigger edges as well as the logic thresholds are programmable in this mode.

Figure 3-10. Front Panel Controls (Continued)


37
FUSE
PULL
~ LINE V
48-440 Hz
VA MAX
FUSE
220V
240V
A TOTAL
+5V
+5V
+5V
36
35

❸❺ The ac power input module permits operation with 100, 120, 220, or 240 volts ac. The number visible in the window indicates nominal line voltage to which instrument must be connected (see *Figure 2-1*). Protective grounding conductor connects to the instrument through this module.

❸❻ This external connector provides three +5V sources to power the HP545A Logic Probe, the HP546A Logic Pulser, the HP547A Current Tracer, or the HP5001A Microprocessor Exerciser.

❸❼ Fuse-Pull.

Figure 3-11. Rear Panel Features

Table 3-5. Operator Checks

OPERATOR CHECKS PROCEDURE

NOTE

Before switching on the instrument, ensure that the voltage selector is set to the correct position, the correct fuse is installed, and the safety precautions, as described in Section II, paragraph 2-5 through 2-11, are observed.

STEP	PROCEDURE	RESULTS
1.	Set 5005A LINE switch to ON.	When the instrument is first turned-on, the microprocessor performs a self-test as indicated by all LEDs lighted for a few seconds. The GATE and UNSTABLE LEDs flash momentarily. After self-test, the 5005A should be in the NORM Signature Analysis mode, with TTL thresholds selected and all positive polarities indicated by the respective LEDs.

NOTE

If during power-up or normal operation, an Error Message is displayed, the 5005A could be defective. Refer to Paragraph 3-34, ERROR MESSAGES, in this section.

2.	Press kΩ ⊡	kΩ ⊙ pushbutton LED lights. 5005A displays O P E N.
3.	Connect Data Probe tip to the Pod START/ ST-SP (green), STOP/ QUAL (red) and CLOCK (yellow) leads sequentially.	5005A measures approximately 100kΩ for each lead.
4.	Connect Data Probe tip to the Pod ground (black) lead.	5005A measures 0±.002.

Table 3-6. NORM Signature Analysis Measurement

NORM SIGNATURE ANALYSIS MEASUREMENT PROCEDURE

NOTE

Correct (expected) signatures for the Device Under Test (DUT) must be known for proper use of the 5005A. Signatures will usually be listed in the troubleshooting section of the DUT manual.

NOTE

The Logic probe is active in this mode.

STEP	PROCEDURE	RESULTS
1.	Press NORM ⊡ .	NORM ⊡ pushbutton lights.
2.	Connect START/ST-SP, STOP/QUAL, CLOCK, and Pod ground (⊥) leads to specified test points of the DUT. (Refer to DUT manual.)	
3.	Set DATA ☐ , CLOCK ☐ , and ST-SP-QL ☐ to the Logic family indicated in DUT manual.	Corresponding LEDs light.

NOTE

If the DUT manual specifies a 5004A Signature Analyzer, select only the preset TTL THRESHOLD levels.

STEP	PROCEDURE	RESULTS
4.	Set CLOCK ☐ , START ☐ , and STOP ☐ edges as stated in DUT manual.	Specified edges toggle and LEDs light. GATE light indicates gating.

Table 3-6. NORM Signature Analysis Measurement (Continued)

NORM SIGNATURE ANALYSIS MEASUREMENT PROCEDURE (Continued)

5.	The set-up can be checked by probing Vcc for an expected signature.	5005A displays Vcc signature.
6.	Connect Data Probe to the tested node of DUT.	5005A displays test signatures to be compared with those in DUT manual.

NOTE

The first two signatures displayed may be wrong, which is noticable when slow gating is used. In this condition the UNSTABLE LED will light and the signatures should be ignored. When a signature, which is different from the preceeding signature is displayed, the UNSTABLE LED lights. The first correct signature (following an incorrect signature) will have the UNSTABLE LED lighted. Only at the second correct signature will the UNSTABLE LED turn-off. The 5005A has to read at least two identical stable signatures before the UNSTABLE LED will turn-off as indicated below.

DISPLAYED SIGNATURE	INCORRECT	INCORRECT	CORRECT	CORRECT	CORRECT
UNSTABLE LED	ON	ON	ON	OFF	OFF

Table 3-7. QUAL Signature Analysis Measurement

QUAL SIGNATURE ANALYSIS MEASUREMENT PROCEDURE

NOTE

Correct (expected) signatures for the Device Under Test (DUT) must be known for proper use of the 5005A. Signatures will usually be listed in the troubleshooting section of the DUT manual.

NOTE

The Logic probe is active in this mode.

STEP	PROCEDURE	RESULTS
1.	Press QUAL ⊡ .	QUAL ⊡ pushbutton lights.
2.	Connect START/ST-SP STOP/QUAL, CLOCK, and Pod ground (⊥) leads to specified test points of the DUT. (Refer to DUT manual.)	
3.	Set DATA ☐ , CLOCK ☐ , and ST-SP-QL ☐ to the Logic family indicated in DUT manual.	Corresponding LEDs light.
4.	Set CLOCK ☐ , START ☐ , STOP ☐ edges and QUAL ☐ level as in DUT manual.	Specified edges toggle and LEDs light. GATE light indicates gating.
5.	The set-up can be checked by probing Vcc for an expected signature.	5005A displays Vcc signature.

Table 3-7. QUAL Signature Analysis Measurement (Continued)

QUAL SIGNATURE ANALYSIS MEASUREMENT PROCEDURE (Continued)

6.	Connect Data Probe to the tested node of DUT.	5005A displays test signatures to be compared with those in DUT manual.

NOTE

The first two signatures displayed may be wrong, which is noticable when slow gating is used. In this condition, the UNSTABLE LED will light and the signatures should be ignored. When a signature, which is different from the preceeding signature is displayed, the UNSTABLE LED lights. The first correct signature (following an incorrect signature) will have the UNSTABLE LED lighted. Only at the second correct signature will the UNSTABLE LED turn-off. The 5005A has to read at least two identical stable signatures before the UNSTABLE LED will turn-off as indicated below.

DISPLAYED SIGNATURE	INCORRECT	INCORRECT	CORRECT	CORRECT	CORRECT
UNSTABLE LED	ON	ON	ON	OFF	OFF

Table 3-8. Frequency Measurement

FREQUENCY MEASUREMENT PROCEDURE

NOTE

The Logic probe is active in this mode.

STEP	PROCEDURE	RESULTS
1.	Press kHz ⊡ .	kHz ☼ pushbutton lights. Gate LED flashes at the fixed 1Hz gating rate.
2.	Set DATA ☐ to desired logic family.	Selected logic family LED lights.
3.	Ensure one of the ground (⊥) leads is connected to the DUT ground. For frequencies above 10MHz, the Data Probe ground (⊥) lead should be used.	

NOTE

The frequency measured gate time is fixed at one second as indicated by the flashing GATE LED at the right of the display.

4.	Place the Data Probe tip on the signal to be measured.	Display shows the measured frequency with the GATE LED flashing at the measurement rate.

Table 3-9. Totalize Measurement

TOTALIZE MEASUREMENT PROCEDURE

NOTE

The Logic probe is active in this mode.

STEP	PROCEDURE	RESULTS
1.	Press TOTLZ ⊡ .	TOTLZ ☼ pushbutton lights.
2.	Set DATA ☐ and ST-SP-QL ☐ to desired logic family.	Selected logic family LEDs light.
3.	Set desired START ☐ and STOP ☐ edges.	Selected edges toggle and LEDs light.
4.	Connect the Pod START/ST-SP and STOP/QUAL leads to the START and STOP signals.	
5.	Connect the Pod ground (⊥) lead to the ground of the DUT.	GATE light indicates gating.
6.	Place the Data Probe tip on the signal to be totalized.	Display shows the number of pulses occurring during the time between the Start and Stop edges.

Table 3-10. Time Interval Measurement

TIME INTERVAL MEASUREMENT PROCEDURE

NOTE

The Logic probe is not active in this mode and any activity by the lamp should be ignored.

STEP	PROCEDURE	RESULTS
1.	Press ms [•] .	ms [☼] pushbutton lights.
2.	Set ST-SP-QL ▢ to desired logic family.	Selected logic family LED lights.
3.	Set desired START ▢ and STOP ▢ edges.	Selected edges toggle and LEDs light.
4.	Connect the Pod ground (⊥) lead to the ground of the DUT.	GATE light indicates gating.
5.	Connect the Pod START/ST-SP and STOP/QUAL leads to the START and STOP signals to be measured.	Display shows the time interval between selected transitions of the START and STOP signals.

Table 3-11. Resistance Measurement

RESISTANCE MEASUREMENT PROCEDURE

NOTE

The Logic probe is not active in this mode and any activity by the lamp should be ignored.

STEP	PROCEDURE	RESULTS
1.	Press $\overset{k\Omega}{\boxed{\bullet}}$.	$\overset{k\Omega}{\boxed{\circ}}$ pushbutton lights. If the Data Probe is not connected, the 5005A displays O P E N.

CAUTION

Before taking resistance measurements ensure the tested circuit is not under power and disconnected from the earth ground. This can normally be done by disconnecting the AC power cord.

2.	Connect Data Probe ground (⊥) lead on one side of resistance to be measured.	
3.	Place Data Probe tip on other side of resistance to be measured.	Display shows the measured resistance between the Data Probe tip and ground.

Table 3-12. Voltage Measurement

VOLTAGE MEASUREMENT PROCEDURE

NOTE

The Logic probe is not active in this mode and any activity by the lamp should be ignored.

STEP	PROCEDURE	RESULTS
1.	Press DCV ⊡.	DCV ☼ pushbutton lights.
2.	Connect Data Probe or Pod ground (⊥) lead to the common ground point of source to be measured.	
3.	Place Data Probe tip on voltage point to be measured.	Display shows the measured voltage between the Data Probe and ground.

CAUTION

The Ground input of the DVM is attached to earth ground via the instrument chassis. Do not connect to any voltage other than earth ground.

Table 3-13. Delta Voltage Measurement

DELTA VOLTAGE MEASUREMENT PROCEDURE

NOTE

The Logic probe is not active in this mode and any activity by the lamp should be ignored.

STEP	PROCEDURE	RESULTS
1.	Connect Data Probe or Pod ground (⊥) lead to the common ground point of source to be measured.	
2.	Place Data Probe tip on circuit point to be used as a voltage reference point. Press Δv ⊡ . Hold Data Probe on voltage reference until a numeric display (≈ 0.000) appears.	Δv ☼ pushbutton lights. 5005A displays zero voltage difference. This is the reference voltage for the following difference measurements.
3.	Place Data Probe tip on the circuit point whose voltage is to be measured.	Display shows the voltage difference between the currently probed circuit point and the previously defined reference (step 2) point.

Table 3-14. Peak Voltage Measurement

PEAK VOLTAGE MEASUREMENT PROCEDURE

NOTE

The Logic probe is not active in this mode and any activity by the lamp should be ignored.

STEP	PROCEDURE	RESULTS
1.	Press $\overset{Vp+}{\boxed{\bullet}}$ or $\overset{Vp-}{\boxed{\bullet}}$.	Selected pushbutton lights.
2.	Connect Data Probe ground (⊥) lead to the ground of test. Leaving the Data Probe ground disconnected will result in inaccurate measurements.	

NOTE

Disregard blinking of GATE LED and Data Probe logic light.

3.	Place Data Probe tip on the circuit point at which peak plus or minus voltage is to be measured.	Display shows the peak voltage value at the Data Probe.

SECTION IV
PERFORMANCE TESTS

4-1. INTRODUCTION

4-2. The procedures in this section test the electrical performance of the 5005A using the specifications in *Table 1-1* as a standard. The first series of tests constitute an Operation Verification, which checks the major functions of the 5005A. This test can be performed to give a high degree of confidence that the 5005A is operating properly. The second series of tests provide a full performance test which tests the instrument against the given specifications. All tests can be performed without access to the inside of the instrument. The operation verification should be useful for incoming QA, routine maintenance, and after instrument repair.

4-3. EQUIPMENT REQUIRED

4-4. The equipment required for the operation verification procedure is listed in *Table 1-2*. Any equipment that satisfies the critical specifications given in the table may be substituted for the recommended model numbers.

4-5. CALIBRATION CYCLE

4-6. The 5005A requires periodic verification of operation. Depending on the use and environmental conditions, the 5005A should be checked using the operation verification procedure at least once every year.

4-7. TEST RECORD

4-8. Results of the Operation Verification Tests may be tabulated on *Table 4-2*; Operation Verification Test Record, located at the end of the procedures. Results of the Performance Test procedures may be tabulated on table 4-3; Performance Test Record.

4-9. OPERATION VERIFICATION PROCEDURES

4-10. Self-Check

a. Before switching on the instrument, ensure that power cord is properly attached, the correct fuse is installed, and that all safety precautions have been observed.

b. Set LINE ON-OFF switch to ON and verify the Self-Check routine as follows: Upon applying power, all front panel LEDs, except for GATE and UNSTABLE, should light momentarily. GATE and UNSTABLE should randomly flash on and off, and the 5005A display should be " -8.8.8.8.8. ". After approximately three seconds, verify that four lighted bars (the center segments of the four rightmost display LEDs) are displayed and the NORM, CLOCK, START, STOP, and all TTL level LED indicators are lighted. Verify that all other LEDs are unlighted. See *Figure 4-1*.

c. Record results on operation verification test record, *Table 4-2*.

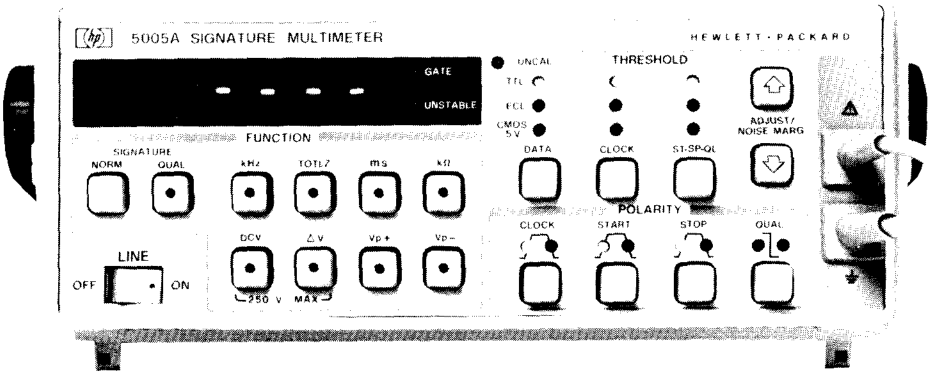

5005A SIGNATURE MULTIMETER
HEWLETT · PACKARD
GATE
UNSTABLE
UNCAL
TTL
ECL
CMOS 5V
THRESHOLD
ADJUST/ NOISE MARG
SIGNATURE
NORM
QUAL
FUNCTION
kHz
TOTLZ
ms
kΩ
DATA
CLOCK
ST-SP-QL
POLARITY
CLOCK
START
STOP
QUAL
LINE
OFF
ON
DCV
ΔV
Vp+
Vp−
250 V MAX

Figure 4-1. Self-Check

4-11. Frequency Counter Verification

a. Proper operation will be checked by applying a signal of a specific frequency and amplitude and verifying that the 5005A displays the correct frequency.

b. Connect equipment as follows:

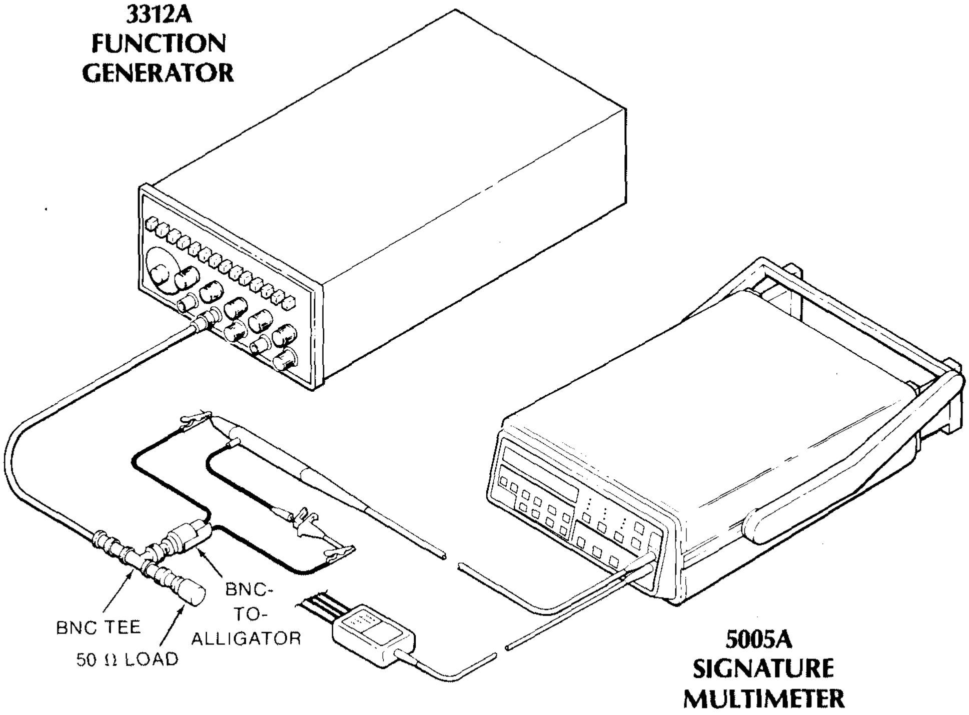

3312A FUNCTION GENERATOR
BNC TEE
50 Ω LOAD
BNC-TO-ALLIGATOR
5005A SIGNATURE MULTIMETER

Figure 4-2. Frequency Counter Operation Verification Test Setup

c. With the 3312A LINE switch to "OFF", press the 5005A front panel **kHz** pushbutton. The display should read " 0.000 ", the GATE LED should flash every second, and DATA THRESHOLD TTL LED should be lighted. All other LEDs should be unlighted.

d. Set the 3312A LINE switch to "ON", and adjust the output for a 10 Hz squarewave with an amplitude of 10V (-5V to +5V).

e. Connect the Data Probe to the 3312A and verify that the 5005A displays ~" 0.010 " with all LED indications the same as in step c. The Data Probe light should be flashing.

f. Set the 3312A to output a 2 MHz squarewave with an amplitude of 10V (-5V to +5V).

g. Connect the Data Probe to the 3312A and verify that the 5005A displays ~" 2000 " with all LED indications the same as in step c. The Data Probe light should be flashing.

h. Record results on operation verification test record, *Table 4-2*.

4-12. Totalizing Counter Verification

a. Proper operation will be checked by applying a signal of a specific frequency and amplitude and verifying that the 5005A displays a correct totalized indication.

b. Connect equipment as follows:

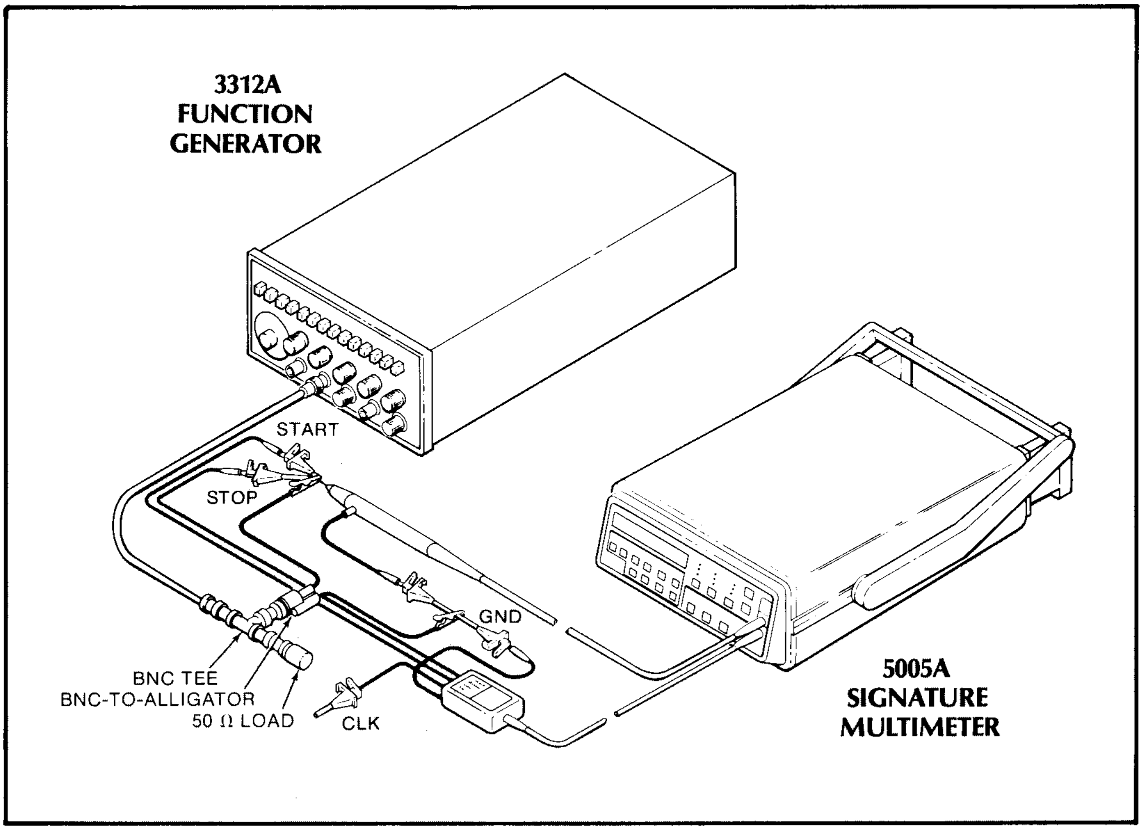


Figure 4-3. Totalizing Counter Operation Verification Test Setup

c. Press the 5005A front panel **TOTLZ** pushbutton. Verify that four lighted bars are displayed, the DATA and ST-SP-QL THRESHOLD TTL, and the POLARITY START and STOP rising edge LEDs are lighted. All other LEDs should be unlighted.

d. Set the 3312A to output a 100 Hz squarewave with an amplitude of 10V (-5V to +5V).

e. Set the START and STOP edge selects to the ⎺\⎽ position.

f. Connect the Data Probe and the START/ST-SP (green) and STOP/QUAL (red) Pod test leads to the 3312A. Verify that the display reads " 0001 " with the GATE LED flashing all other LED indications the same as in step c.

g. Record results on operation verification test record, *Table 4-2.*

4-13. Time Interval Verification

a. Proper operation will be checked by applying a signal of a specific frequency and amplitude and verifying that the 5005A displays the correct time interval indication.

b. Connect equipment as follows:

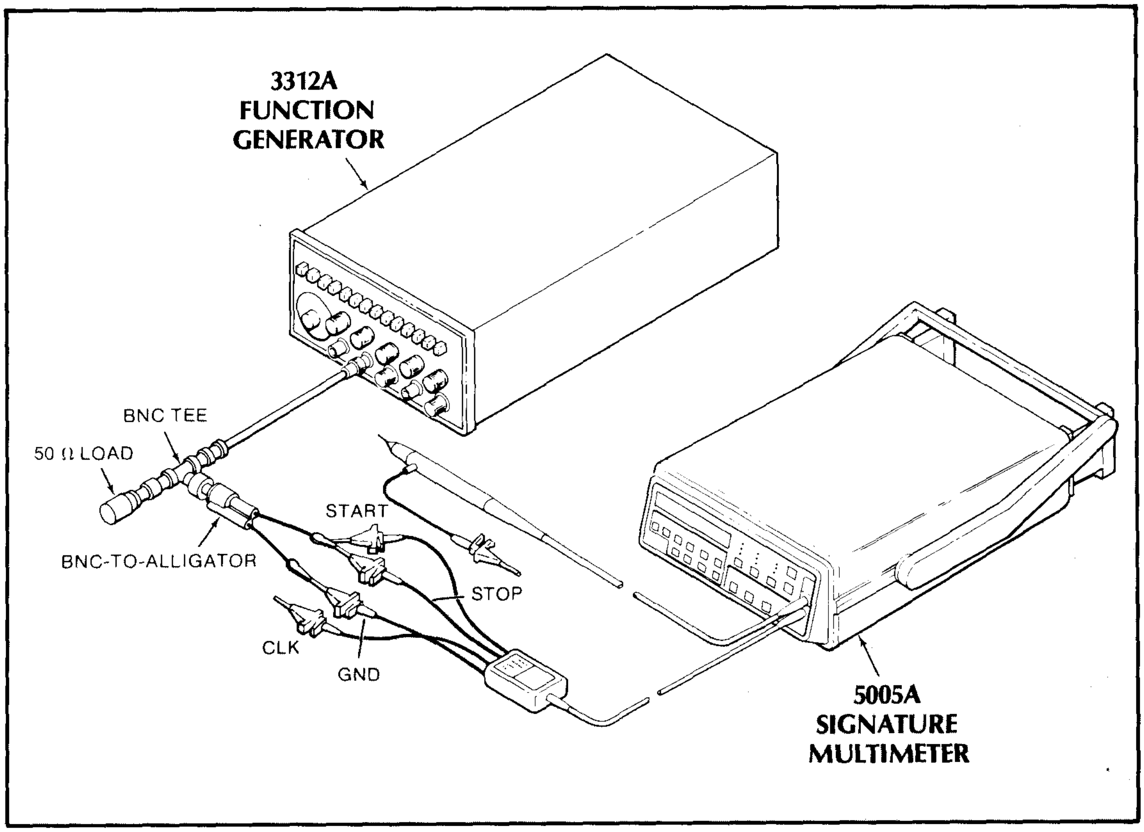


Figure 4-4. Time Interval Operation Verification Test Setup

c. Press the 5005A front panel **ms** pushbutton. Verify that four lighted bars are displayed, the SP-ST-QL, THRESHOLD TTL, and POLARITY START and STOP rising edge LEDs are lighted. All other LEDs should be unlighted.

d. Set the 3312A to output a 100 Hz squarewave with an amplitude of 10V (-5V to +5V).

e. Verify that the START and STOP edge selects are set to the ⎽/⎺ position.

f. Connect the Data Probe and the START/ST-SP (green), and STOP/QUAL (red) Pod test leads to the 3312A. Verify that the display reads ~" 10. " ms with the GATE LED flashing and all other LED indications the same as in step c.

g. Record results on operation verification test record, *Table 4-2.*

4-14. Ohmmeter Verification

a. Proper operation will be checked by connections from the Data Probe to the Pod, verifying the ground continuity and input impedance in the Pod, and in the Data Probe.

b. Press the 5005A front panel **kΩ** pushbutton. With the Data Probe **not** connected, verify that the kΩ LED is lighted and the display reads " OPEN ".

c. Connect the equipment as follows:

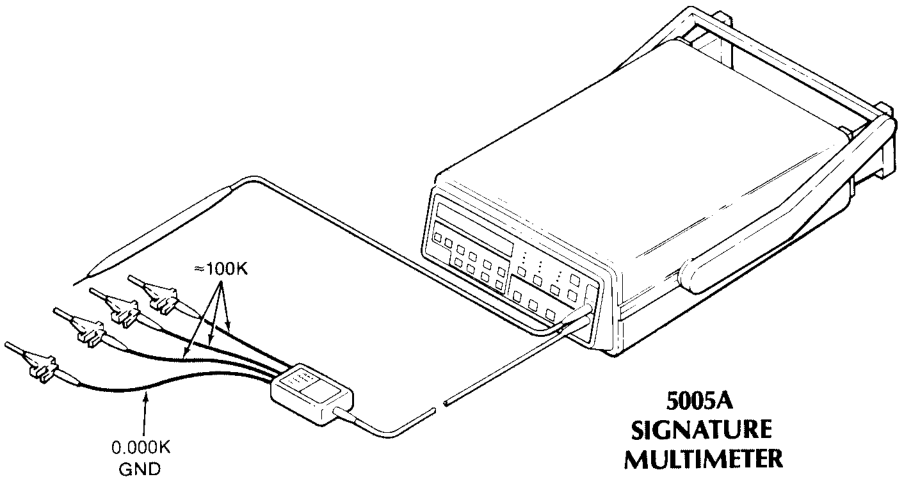


Figure 4-5. Ohmmeter Operation Verification Test Setup

d. Connect the Data Probe tip to the Pod ground (⊥) connector. Verify that the display reads "0.000" ±0.002.

e. Connect the Data Probe tip to the Pod START/ST-SP, STOP/QUAL, and CLOCK test leads sequentially. Verify that the display reads ~" 100 " kΩ for each connection.

f. Connect the Data Probe tip to the Data Probe ground (⊥) connector. Verify that the display reads "0.0000" ±0.002.

g. Record results on operation verification test record, *Table 4-2*.

4-15. Voltmeter Verification

a. Proper operation will be checked by activating the voltage buttons and verifying the correct display and LED indications.

b. Connect equipment as follows:

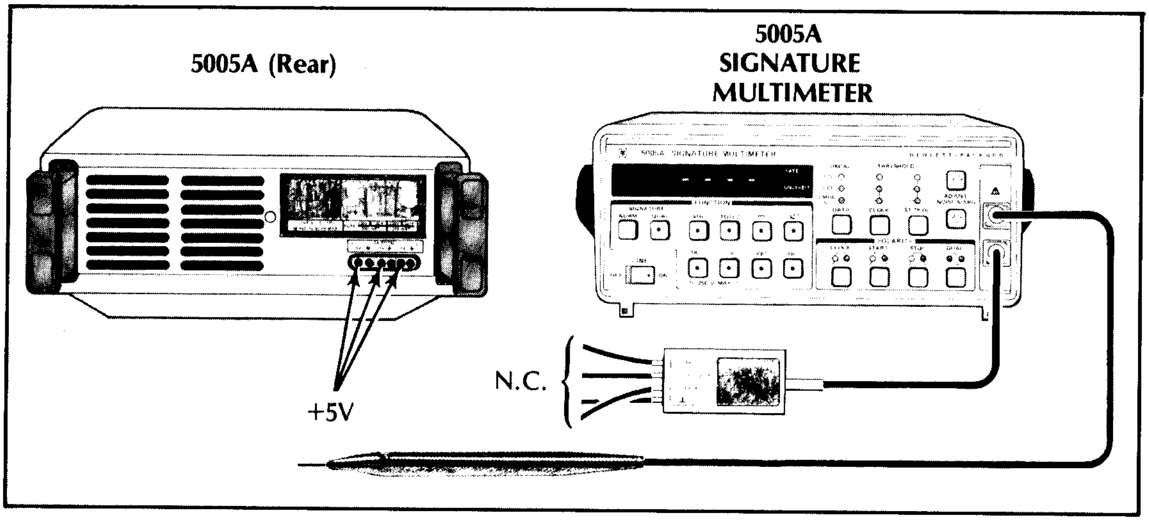


Figure 4-6. Voltmeter Operation Verification Test Setup

c. With the Data Probe grounded, press the 5005A front panel **DCV** pushbutton. Verify that the display reads "0.000" ±0.002.

d. With the Data Probe grounded, press the 5005A front panel **Vp+** pushbutton. Verify that the display reads "0.00" ±0.05 and the GATE light flashes.

e. With the Data Probe grounded, press the 5005A front panel **Vp-** pushbutton. Verify that the display reads "0.00" ± 0.05.

f. With the **Vp-** pushbutton activated, connect the Data Probe to +5V and ground (⊥) at connector J2 on the 5005A rear panel. Verify display reads "5.00" ± 0.5.

NOTE

Perform the following tests with the Data Probe connected as in step f.

g. Press the 5005A front panel **Vp+** pushbutton. Verify that the display reads "5.00" ± 0.5.

h. Press the 5005A front panel **ΔV** pushbutton. Verify that the display reads "0.000" ± 0.5.

i. Place the probe on ⊥ and verify that the display reads "-5.00" ±0.5.

j. Press the 5005A front panel **DCV** pushbutton. Verify that the display reads "5.000" ±0.300.

k. Record results on operation verification test record, *Table 4-2.*

4-16. Signature Analysis Verification

4-17. The following tests verify the signature analysis circuits of the 5005A. If a 5036A Microprocessor Lab is not available, any instrument with documented signature analysis capability can be used. Connect the 5005A pod connectors as described in the substitute instrument's manual, and verify a documented signature. When using a substitute instrument for the 5036A, only the NORM mode of signature analysis can be verified unless the qualifier input is specified by the unit under test.

4-18. NORMAL Mode Verification

a. Proper operation will be checked by connecting the 5005A Signature Multimeter and 5036A Logic Lab and verifying correct signatures.

b. Set the 5005A LINE ON-OFF switch to ON. With the 5036 LINE switch to "OFF", verify that four lighted bars are displayed, and the NORM, CLOCK, START, STOP, and all TTL level LED indicators are lighted. Verify that all other LEDs are unlighted.

c. Set the 5036A LINE ON-OFF switch to ON. Verify the ADDRESS/REGISTER and DATA LEDs read " 8888 88 " momentarily, then " uLA8 UP ". Refer to *Figure 4-10.*

d. Set the 5036A LINE ON-OFF switch to OFF.

e. Set the 5036A switches as follows:

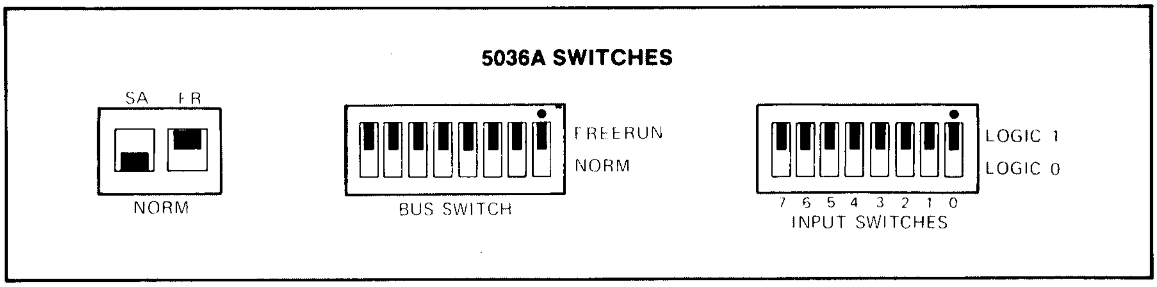


Figure 4-7. Signature Analysis, NORMAL Mode Switch Setting

f. Connect the equipment as follows:

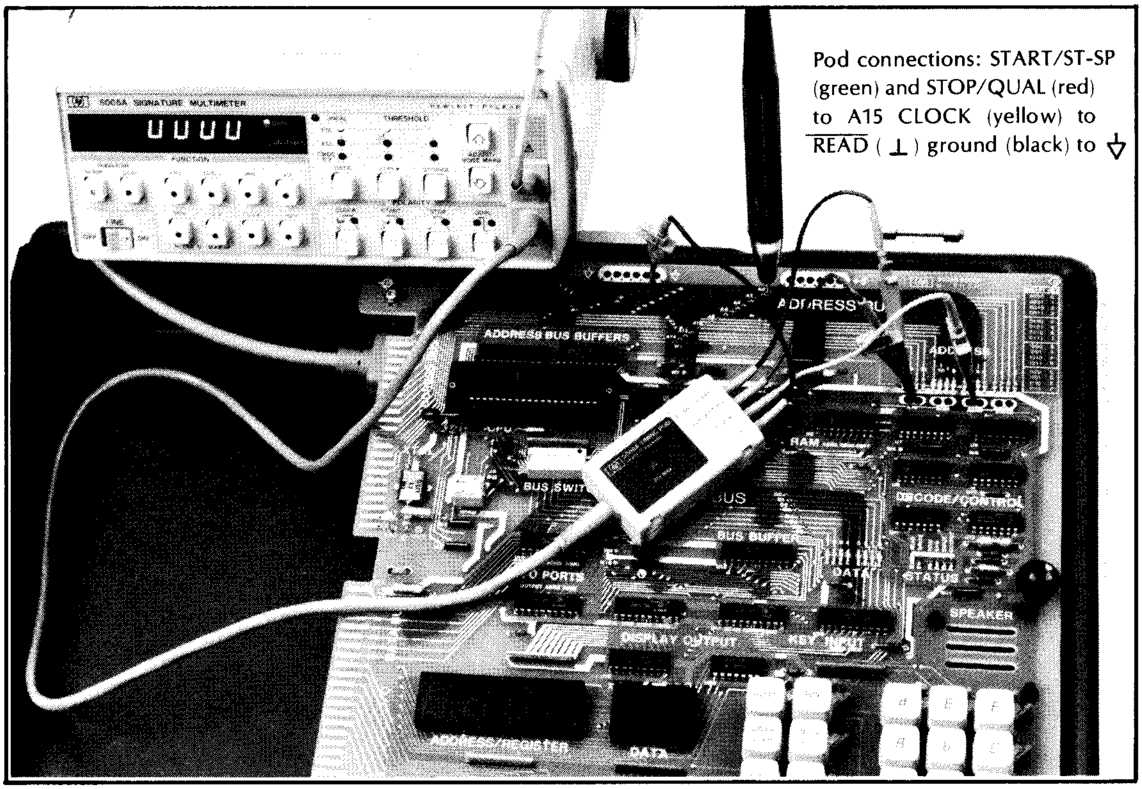

Pod connections: START/ST-SP (green) and STOP/QUAL (red) to A15 CLOCK (yellow) to $\overline{\text{READ}}$ (⊥) ground (black) to ⏚

Figure 4-8. Signature Analysis, NORMAL Mode Operation Verification Test Setup

g. Set the 5036A LINE ON-OFF switch to ON. Verify the ADDRESS LEDs are lighted with two LEDs blinking.

h. Connect the Data Probe to a +5 volt test connection. Refer to *Figure 4-10*. Verify that the 5005A display reads " *0001* " with the GATE LED flashing and all other LED indications are the same as in step b.

i. Connect the Data Probe to test point A0 (ADDRESS BUS). Refer to *Figure 4-10*. Verify that the 5005A display reads " *UUUU* " with the GATE LED flashing and all other LED indications are the same as in step b.

j. Set the 5005A and 5036A LINE ON-OFF switches to OFF, disconnect test equipment, and reconfigure the 5036A switches to their original positions. Record results on operation verification test record, *Table 4-2*.

4-19. QUAL Mode Verification

a. Proper operation will be checked by connecting the 5005A Signature Multimeter and 5036A Logic Lab and verifying correct signature indications.

b. Set the 5005A LINE ON-OFF switch to ON.

c. Set the 5036A LINE switch to "OFF". Press the SIGNATURE QUAL pushbutton. Press the POLARITY QUAL pushbutton, to toggle the qualifier to the low level position. Verify that four lighted bars are displayed, and the QUAL, CLOCK, START, STOP, QUAL (falling edge), and all TTL level indicators are lighted. Verify that all other LEDs are unlighted.

d. Repeat steps 4-18, c through e.

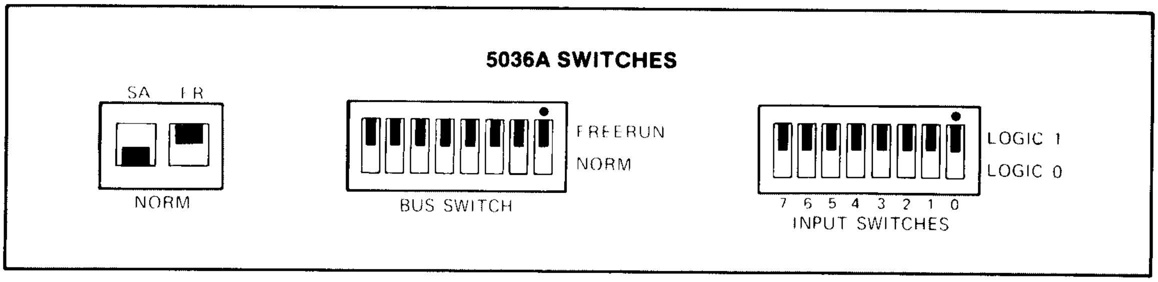


Figure 4-9. Signature Analysis, QUAL Mode Switch Settings

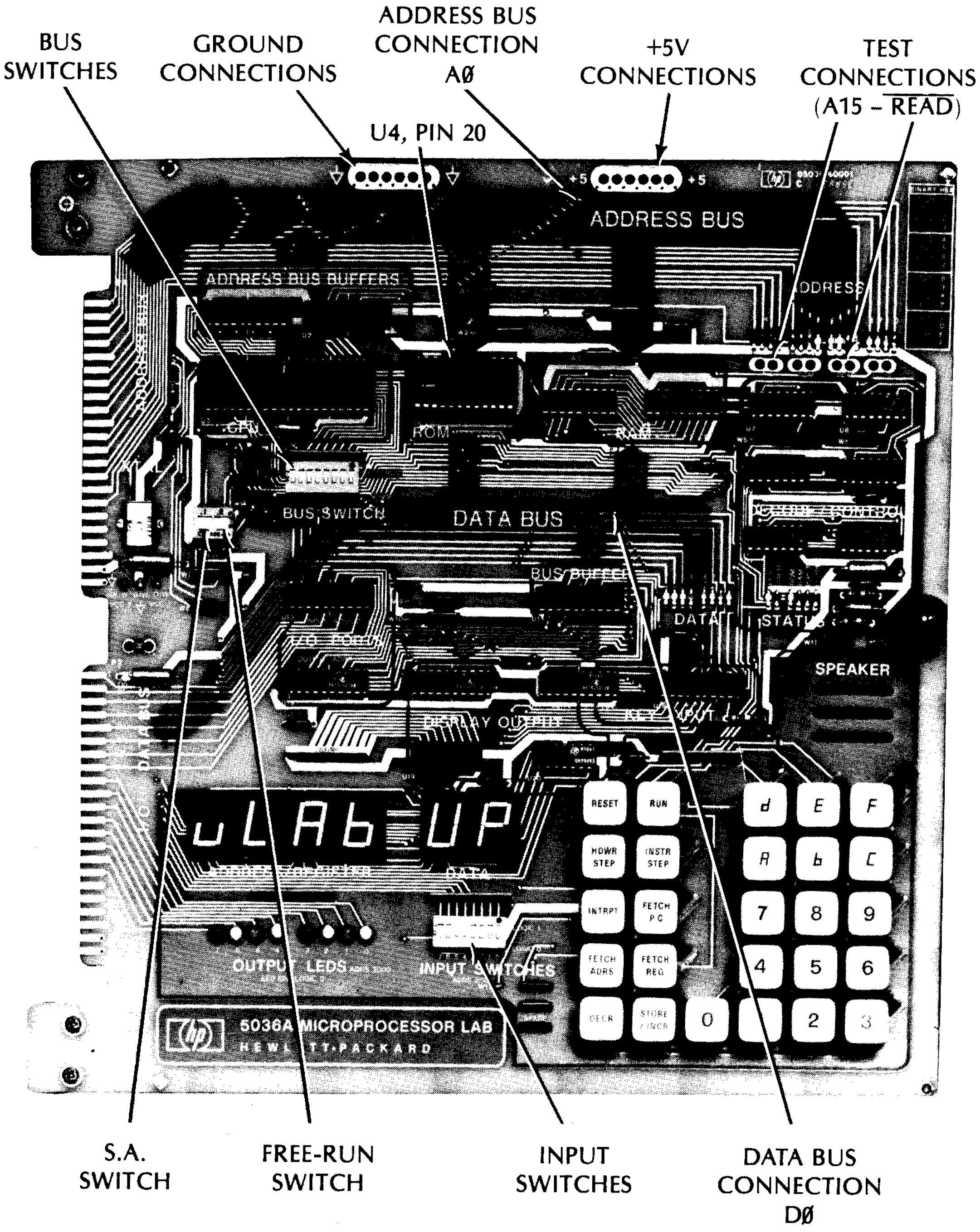

BUS SWITCHES
GROUND CONNECTIONS
ADDRESS BUS CONNECTION A0
U4, PIN 20
+5V CONNECTIONS
TEST CONNECTIONS (A15 – $\overline{\text{READ}}$)
ADDRESS BUS
ADDRESS BUS BUFFERS
CPU
ROM
RAM
BUS SWITCH
DATA BUS
BUS BUFFER
I/O PORTS
DATA
STATUS
SPEAKER
DISPLAY OUTPUT
KEY INPUT
ADDRESS/REGISTER
DATA
OUTPUT LEDS
INPUT SWITCHES
5036A MICROPROCESSOR LAB
HEWLETT-PACKARD
RESET
RUN
HDWR STEP
INSTR STEP
INTRPT
FETCH PC
FETCH ADRS
FETCH REG
DECR
STORE /INCR
S.A. SWITCH
FREE-RUN SWITCH
INPUT SWITCHES
DATA BUS CONNECTION D0

Figure 4-10. 5036A Test Switches and Connection Points

e. Connect the equipment as follows:

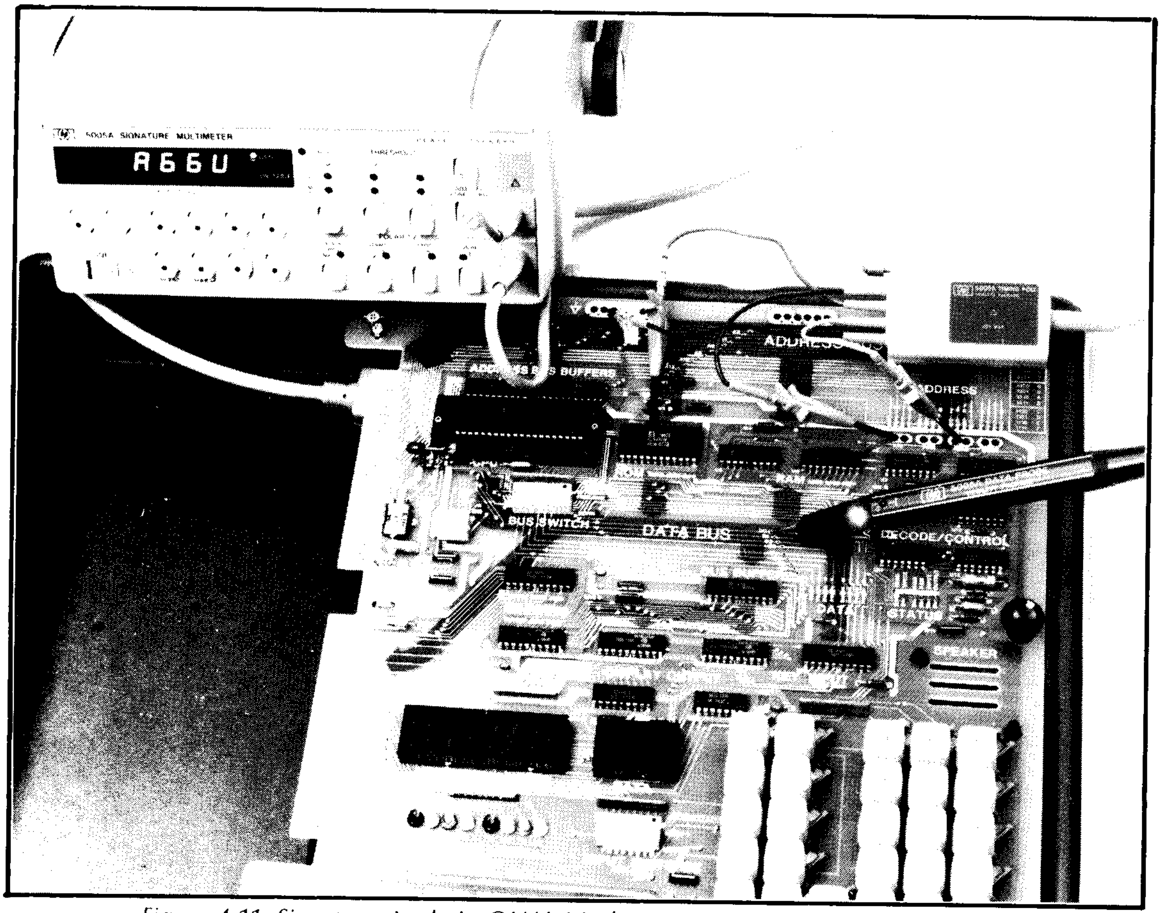

5005A SIGNATURE MULTIMETER
A66U
ADDRESS BUS BUFFERS
ADDRESS
BUS SWITCH
DATA BUS
DECODE/CONTROL
DATA
STATUS
SPEAKER

Figure 4-11. Signature Analysis, QUAL Mode Operation Verification Test Setup

Pod connections:	START/ST-SP (green) to A15 STOP/QUAL (red) to U4 pin 20 CLOCK (yellow) to $\overline{\text{READ}}$ (⊥) ground (black) to ⏚

f. Set the 5036A LINE ON-OFF switch to ON. Verify the ADDRESS LEDs are lighted with two LEDs blinking.

g. Connect the Data Probe to a +5 volt test connection. Refer to *Figure 4-10*. Verify the 5005A display reads " 7A70 " with the GATE LED flashing and all other LED indications the same as in step c.

h. Connect the Data Probe to test point D0 (DATA BUS). Refer to *Figure 4-10*. Verify that the 5005A display reads " A66U " with the GATE LED flashing and all other LED indications the same as in step c.

i. Set the 5005A and 5036A LINE ON-OFF switches to OFF, disconnect test equipment, and reconfigure the 5036A switches to their original positions. Record results on operation verification test record, *Table 4-2*.

4-20. PERFORMANCE TEST PROCEDURES

4-21. RESISTANCE Performance Test (kΩ)

Specification:

Range	Accuracy	Resolution
30 kΩ	±1% of reading ±2Ω	1Ω
300 kΩ	±1% of reading	10Ω
1 MΩ	±1% of reading	100Ω
3 MΩ	±10% of reading	1 kΩ
10 MΩ	±10% of reading	10 kΩ

Description: The following procedure is designed to test the 5005A resistance measurement capability over a sufficient range to guarantee specified accuracy. Several resistors in specified ranges are selected and measured using a high accuracy ohmmeter. Once the true reference values of the resistors are established, the allowable measurement tolerance values are computed using the Accuracy specification listed above. Each resistor is then measured by the 5005A. All measurements should fall within the calculated limits.

Equipment:

6 resistors	see range chart
Precision Ohmmeter	3455A,3456A,3490A

Procedure:

1. Obtain six resistors with labeled dc resistance values in the following ranges:

   75 — 150 ohm
   10k — 20k ohm
   100 — 200k ohm
   500k — 700k ohm
   1.5M — 2.0M ohm
   4.0M — 7.0M ohm

2. Using a high precision ohmmeter, measure the actual value of each of the six resistors, to five significant digits. Record these reference values on the Test Record.

   If a 3455A is used, use the 2 wire input and set the front panel controls as follows:

Function	2 WIRE kΩ
Auto Cal	ON
Trigger	INTERNAL
Range	AUTO
Math	OFF

3. Calculate the allowable measurement tolerance for each resistor, using the range accuracy specification listed above. For example:

Resistor Measures	Range Multiplier	Allowable Tolerance
130.4 ohms	±1%=±1.3 ohms ±2 ohms	127.1 to 133.7 ohms

   Record a tolerance range for each resistor on the Test Record.

4. Set the 5005A LINE switch to ON, and function to kΩ. Check that the display reads "O P E N" when the probe is not connected to a resistive load.

5. Measure the values of each the six resistors using the 5005A. Record the results on the Test Record. Verify that the measured resistances are within the listed tolerances.

4-22. DC VOLTAGE Performance Test (DCV)

Specification:

Range	Accuracy	Resolution
25V	±0.1% of reading ±2 mV	1 mV
250V (<100V)	±0.25% of reading ±20 mV	10 mV
250V (>=100)	±0.25% of reading ±20 mV	100 mV

Description: The following procedure is designed to test the 5005A DC Voltage measurement capability over a sufficient range to guarantee specified accuracy. The procedure consists of selecting and verifying several dc voltages, representative of the 5005A's DCV input range. The allowable measurement tolerance is computed using the Accuracy specification listed above. Each voltage value is then measured by the 5005A. All measurements should fall within the calculated limits.

Equipment:

Precision Voltmeter	3455A,3456A,3490A
DC Power Supply, Adjustable ±300V	6209B

Procedure:

1. Adjust the power supply to output -250.0 volts. Verify the value by measuring the dc voltage with the precision voltmeter. Record the measurement as a reference, on the Test Record.

   If the HP 3455A is used, set the controls as follows:

Function	⎓ V
Auto Cal	ON
Trigger	INTERNAL
Range	AUTO
Math	OFF

2. Calculate the allowable measurement tolerance, using the range accuracy specification listed above. For example:

Measured Voltage	Range Tolerance	Allowable Tolerance
-250.2	±.25% of reading ±20 mv	249.55 to 250.85

   Record the allowable measurement tolerance on the Test Record.

3. Set the 5005A for DCV. Measure the dc voltage with 5005A, and record the results. Verify that the 5005A's measured value is within the computed tolerances.

4. Repeat the procedure for each of the voltages listed below, alternately measuring the value with the precision voltmeter, computing the allowable measurement tolerance, then measuring again with the 5005A. Record each measurement on the Test Record. All measurements should fall within the indicated tolerances.

Source Voltage	Allowable Tolerance
-250.0V	-250.7 to -249.3
-27.00V	-27.09 to -26.91
-5.000V	-5.007 to -4.993
0.000V	-0.002 to +0.002
+5.000V	+4.993 to +5.007
+27.00V	+26.91 to +27.09
+250.0V	+249.3 to +250.7

4-23. PEAK VOLTAGE Performance Test (Vp+, Vp-)

Specification:

Range	Accuracy	Resolution
0 to ±12 Vp	±2% of reading ±5% of p-p signal ±100 mV	50 mV

Description: The following procedure is designed to test the 5005A's ability to measure voltage peaks on an input signal to the indicated specifications. Initially, a dc reference level is established. The test equipment and input signal are calibrated to the reference level. The peak voltage of the input pulse waveform is then measured with the 5005A and verfied to be within the given tolerances. The entire procedure is then repeated to test the negative peak function.

Equipment:

Precision Voltmeter	3455A,3456A,3490A
DC Power Supply, Adjustable ±5 V	6216A
Pulse Generator, 10 V p-p output	8013A,8012A,8011A
Oscilloscope, 275MHz	1725A

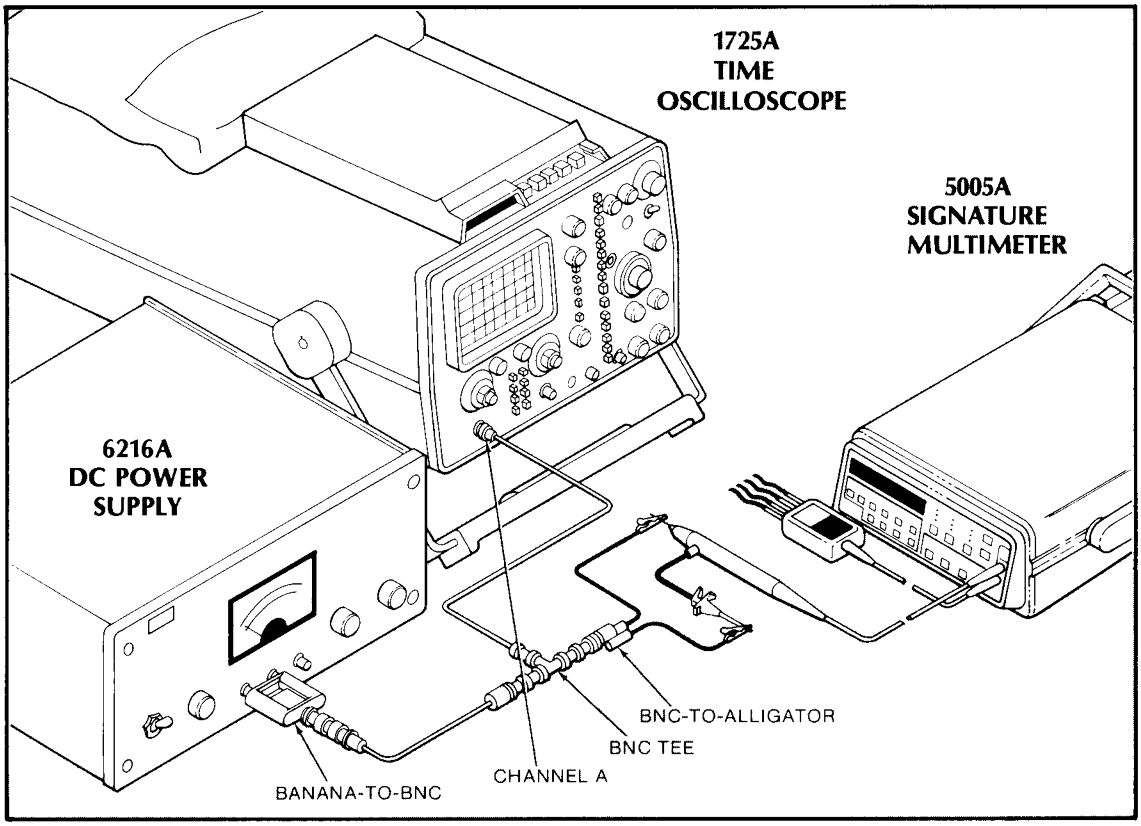


Figure 4-12. Peak Voltage Reference Test Setup

Procedure:

1. Connect the equipment as shown in *Figure 4-12.*
2. Set the dc power supply for a +5.00V output. Use the Precision Voltmeter to adjust the power supply within ±10 mv. Disconnect the voltmeter.
3. With the dc power supply Hi (+5 V) connected to the (DC Coupled) A Channel input of the oscilloscope, adjust the oscilloscope's vertical position control to place the +5 V trace on a reference line. Disconnect the power supply.

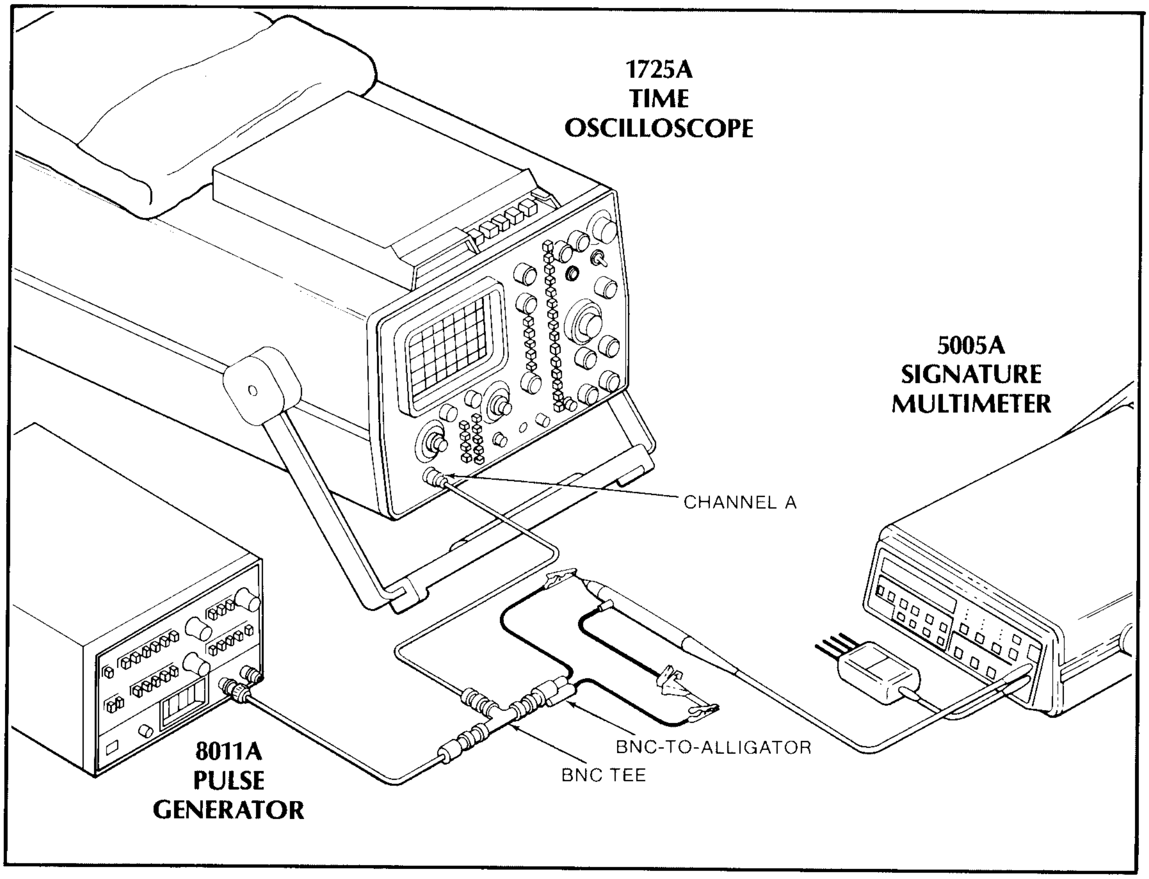
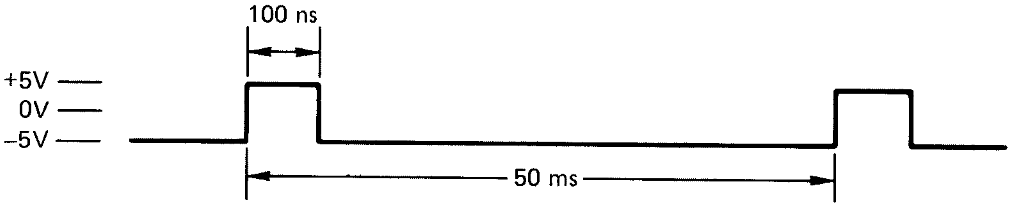

1725A
TIME
OSCILLOSCOPE
5005A
SIGNATURE
MULTIMETER
CHANNEL A
8011A
PULSE
GENERATOR
BNC-TO-ALLIGATOR
BNC TEE

Figure 4-13. Peak Voltage Measurement Test Setup

4. Connect the pulse generator to the A Channel of the oscilloscope. Set the pulse generator to output a 100 ns positive pulse, at a 20 kHz rep rate, with an amplitude of 10 V p-p, as shown below.


100 ns
+5V
0V
−5V
50 ms

5. Adjust the pulse generator to set the peak voltage of the pulse waveform at the +5 V reference level set on the oscilloscope. Disconnect the pulse generator.
6. Connect the pulse generator output to the 5005A Probe, using a BNC-to-alligator connector. Be sure to connect the Probe GND to ground. Set the 5005A function to Vp+, and measure the signal.
7. Verify that the 5005A display is between +4.60 V and +5.40 V. Record the results on the Test Record.
8. Repeat steps one through five, substituting -5 V for +5 V, negative for positive, and -Vp for +Vp.
9. Verify that the 5005A display is between -4.60 V and -5.40 V. Record the results on the Test Record.

4-24. DIFFERENTIAL VOLTAGE Performance Test (ΔV)

Specification:

Range	Accuracy	Resolution
25V	±0.1% of reading ±2 mV	1 mV
250V (<100V)	±0.25% of reading ±20 mV	10 mV
250V (>=100)	±0.25% of reading ±20 mV	100 mV

NOTE

Accuracy is valid as per specification for 1 minute after ΔV key depression.

Description: The following procedure is designed to test the 5005A Differential Voltage measurement capability over a sufficient range to guarantee specified accuracy. The procedure consists of establishing reference voltages, then measuring a representative sampling of voltages within the 5005's range. All the difference measurements should fall within given tolerances of the reference.

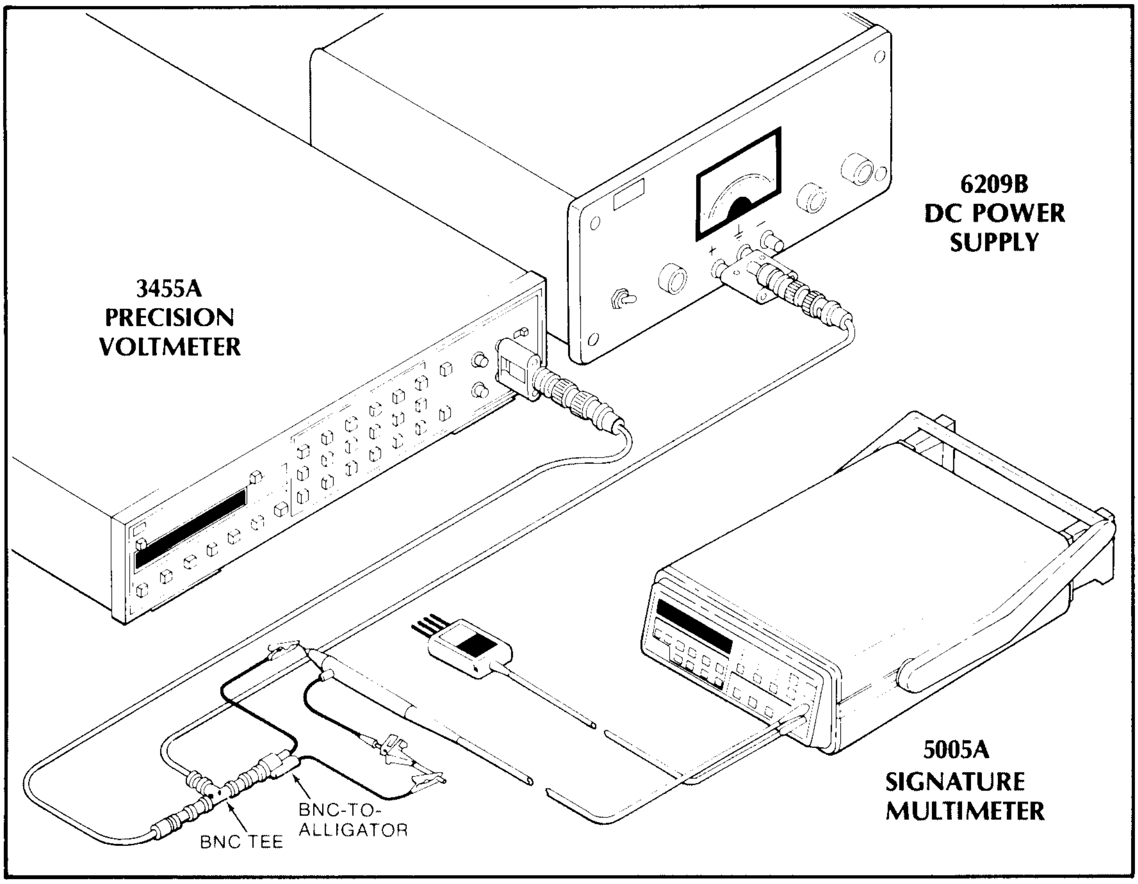


Figure 4-14. ΔD V Test Setup

Equipment:

Precision Voltmeter 3455A,3456A,3490A
DC Power Supply, -300V to +300V 6209B

Procedure:

1. Set the dc power supply to +250.00 V. Verify the voltage within 10 mV, by measuring with the precision voltmeter. Note that the voltmeter and the 5005A can be connected in parallel. If a 3455A is used, set the controls as follows:

   Line .... ON
   Range .... AUTO
   Function .... —V
   Auto Cal .... ON
   Trigger .... INTERNAL
   Math .... OFF

2. After the accuracy of the voltage reference is verified, place the 5005A Probe tip on the positive output of the dc power supply, and connect the GND lead to negative output. Press and hold the ΔV key on the 5005A for about 2 seconds, until a numeric display (≈0.00) appears. This indicates that the Probe tip voltage (+250.0 0V), is stored as a starting reference for the differential measurements to come.

NOTE

It may be necessary to reset the reference between measurements to remain under the 1 minute time limit accuracy specification. The reference voltage accuracy is only valid for one minute.

3. With the 5005A still connected, step the dc power supply through the four voltages listed below. Ensure the 5005A displays a differential measurement within tolerances listed. Record the results on the Test Record.

Probe Tip Reference	dc Power Supply	5005A ΔV Measurement	Allowable Tolerance
+250.0	+200.0	-50.00	±125 mV ± 20 mV
	+10.00	-240.0	±600 mV ±20 mV
	-50.00	-300.0	±750 mV ±20 mV
	-250.0	-500.0	±1.25 V ±20 mV

4. Set the dc power supply for -15.00 V. Repeat steps 1 and 2, establishing -15.00 V as the Probe tip reference. Step the dc power supply through the four voltages listed below. Ensure the 5005A displays a differential measurement with the tolerances listed. Record the results on the Test Record.

Probe Tip Reference	dc Power Supply	5005A ΔV Measurement	Allowable Tolerance
-15.00	-20.00	-5.000	±5 mV ±2 mV
	0.000	+15.000	±15 mV ±2 mV
	+20.00	+35.00	±35 mV ±2 mV
	-10.00	+5.000	±5 mV ±2 mV

Procedure:

4-25. FREQUENCY Performance Test (kHz)

Specification:

Range	Accuracy	Resolution
100 kHz	±0.01% of reading ±1 count	1 Hz
1 MHz	±0.01% of reading ±1 count	1 LSD
10 MHz	±0.01% of reading ±1 count	1 LSD
50 MHz	±0.01% of reading ± count	1 LSD

Description: The following procedure is designed to test the 5005A's frequency measurement capability over a sufficient range to guarantee specified accuracy. The procedure consists of measuring three frequencies; one at the low, middle, and high end of the 5005's input frequency range. A pulse generator is used to produce frequencies which both the 5005A and a high performance frequency counter can measure. The high performance frequency counter's measurement is used as a reference. The allowable measurement tolerance values are computed using the Specification formulas. Each 5005A frequency measurement should fall within the calculated limits.

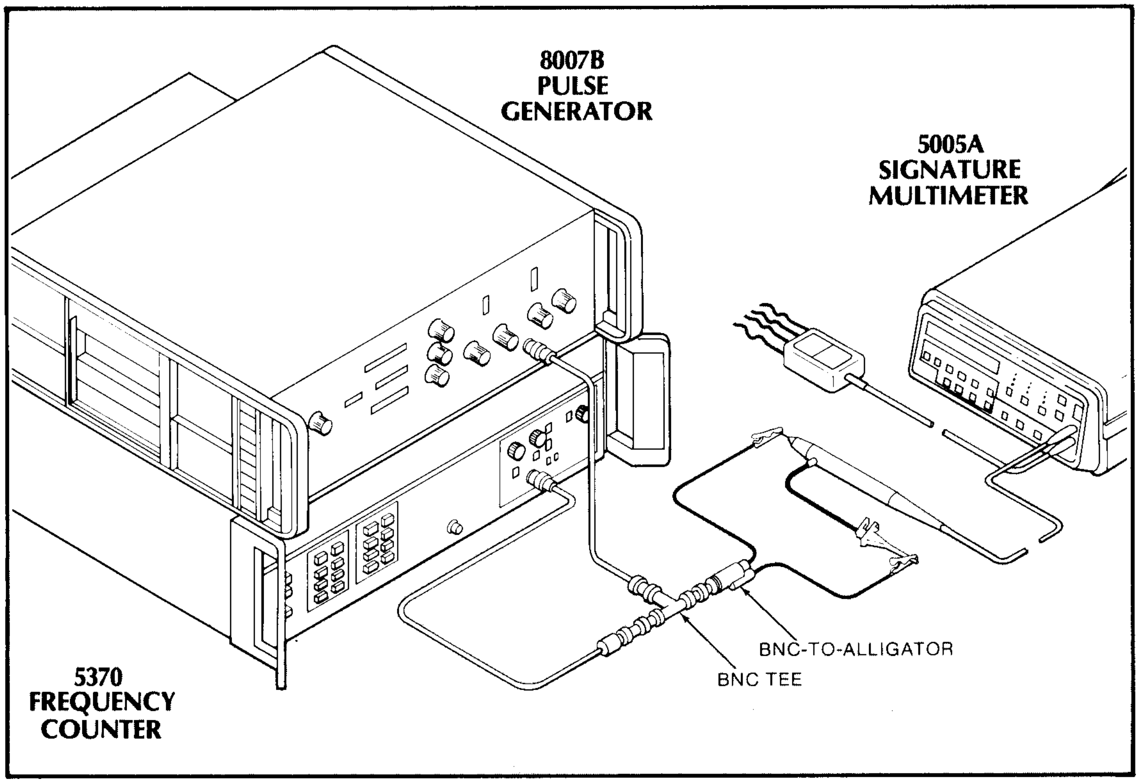


Figure 4-15. Frequency Test Setup

Equipment:

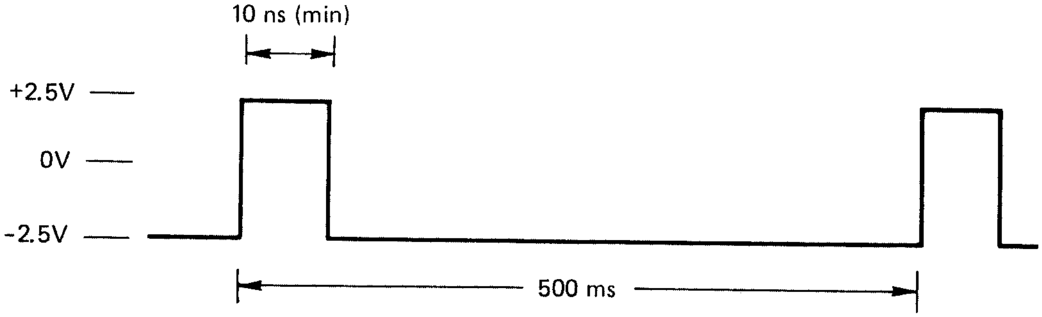
Pulse Generator, 50 MHz	8012A,8013A,8007B
Frequency Counter, 50 MHz	5370A,5316A

Optional Equipment:

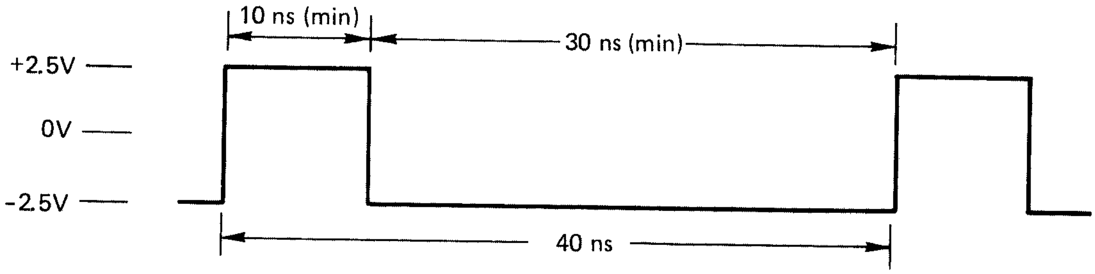
100 MHz oscilloscope	1720A

Procedure:

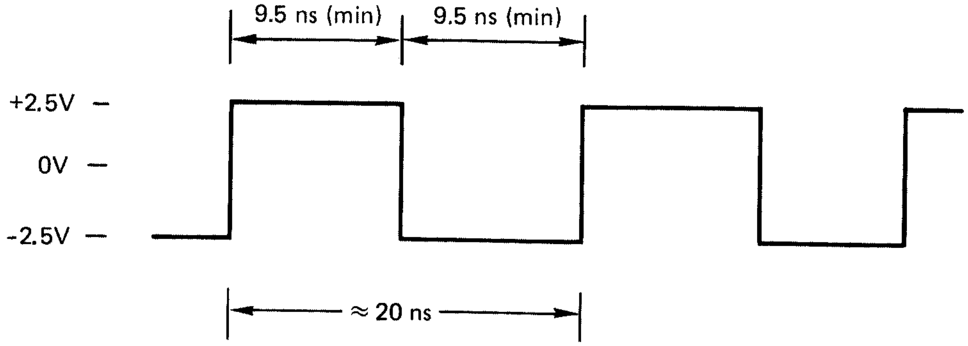
1. Set the pulse generator to output a 2 Hz waveform, five volts p-p, with a duty cycle as shown below. Verify the frequency, using the high performance frequency counter.



2. Place the 5005A in the frequency mode (kHz), with both Lo and Hi Thresholds set to 0.00 volts.
3. With the 5005A Data Probe, measure the frequency of the pulse generator. Compare the 5005A measurement to the high precision frequency counter's measurement. The maximum allowable measurement error at 2 Hz is ± 1 count. Record the results on the Test Record.
4. Set the pulse generator to output a 25 MHz waveform, five volts p-p, with a duty cycle as shown below. Verify the frequency, using the high performance frequency counter.



5. With the 5005A Data Probe, measure the frequency of the pulse generator. Compare the 5005A measurement to the high precision frequency counter's measurement. The maximum allowable measurement error at 25 MHz is ± 4 counts. Record the results on the Test Record.
6. Set the pulse generator to output a 50 MHz waveform, five volts p-p, with a duty cycle as shown below. Verify the frequency, using the high performance frequency counter.



7. With the 5005A Data Probe, measure the frequency of the pulse generator. Compare the 5005A measurement to the high precision frequency counter's measurement. The maximum allowable measurement error at 50 MHz is ± 6 counts. Record the results on the Test Record.

4-26. TOTALIZING Performance Test (TOTLZ)

Specification:

Range	Accuracy	Resolution
0 to 99,999 counts	±1 count	1 count

Description: The following procedure is designed to test the 5005A totalizing measurement capability over a sufficient range to guarantee specified accuracy. The Timing Pod Start and Stop inputs control the 5005A's gate during the totalize mode. These inputs are connected through simple slide switches, to logic low and high TTL levels. The procedure directs the gate to be manually operated via the switches. The gate is opened, a specified number of pulses are input through the Data Probe, and then the gate is closed. This is performed with three representative quanities of pulses. All totalize measurements should fall within ± 1 count of the input amount.

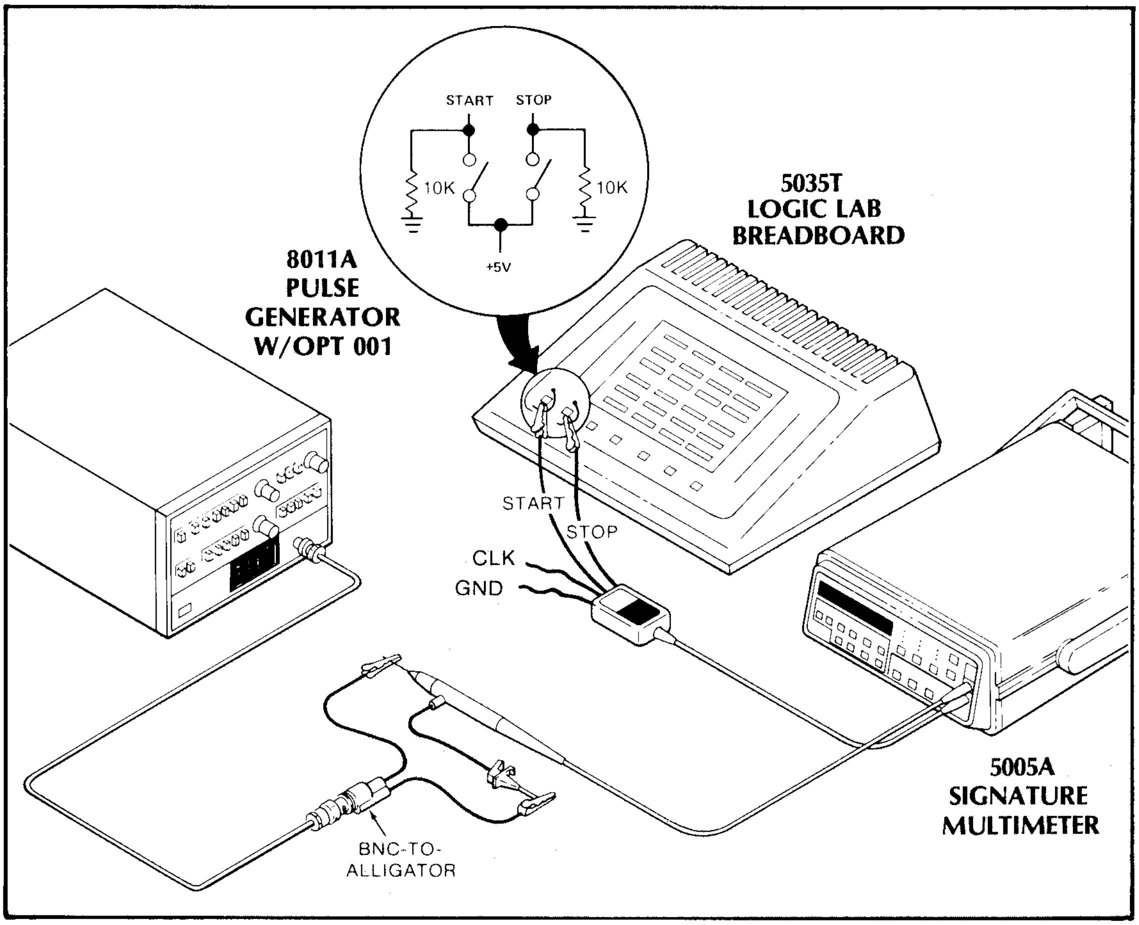

START
STOP
10K
10K
+5V
5035T
LOGIC LAB
BREADBOARD
8011A
PULSE
GENERATOR
W/OPT 001
START
STOP
CLK
GND
BNC-TO-
ALLIGATOR
5005A
SIGNATURE
MULTIMETER

Figure 4-16. Totalize Test Setup

Equipment:

Pulse Generator	8011A/with Option 001

Optional Equipment:

Logic Lab Breadboard	5035T

Procedure:

1. Set the pulse generator up to output a preselected number of pulses in a burst. If a 8011A is used, set the controls as follows:

Period	2 μ - .1 m
Vernier	Fully CCW
Amplitude	0 - 4 V
Vernier	Fully CW
Sym	IN
Burst	ON
Pulse Width	25 n - 1 μs
Vernier	Fully CCW
Number of Pulses	Per Procedure

2. Place the 5005A in the totalize mode (TOTLZ), with Thresholds set to TTL Levels.
3. On the pulse generator, set the number of pulses in the burst to 0001.
4. Move SW1 on the 5035T breadboard from Lo to Hi to Lo. Verify that the GATE LED lights on the 5005A.
5. Press the single burst button on the pulse generator to input the pulses to the 5005A. The Data Probe should light momentarily.
6. Move SW2 from Lo to Hi to Lo. Verify that the GATE LED goes off and the 5005A displays 0001. Record the results on the Test Record.
7. Repeat steps 3 through 6 for pulse burst values of 50,000 and 99,999. Note that the burst must be sent several times within the gate period. Refer to Table 4-1 for procedures. All measurements should match the input burst number. Record the results on the Test Record.

Table 4-1. Totalizing Procedure

# of Pulses	To Obtain	Expected Display
1	Set open gate, number of pulses to 0001. Press single burst, close gate.	0001
50,000	Open gate, set number of pulses to 9999, press single burst 5 times, set number of pulses to 0005, press single burst, close gate.	50,000
99,999	Open gate, set number of pulses to 9999, press single burst 10 times, set number of pulses to 0009, press single burst, close gate.	99,999

4-27. TIME INTERVAL PERFORMANCE TEST (ms)

Specification:

Range	Accuracy	Resolution
10 ms	±0.01% of reading ±1 count	100 ns
100 ms	±0.01% of reading ±1 count	1 count
1 s	±0.01% of reading ±1 count	1 count
10 s	±0.01% of reading ±1 count	1 count
100 s	±0.01% of reading ±1 count	1 count

Description: The following procedure is designed to test the 5005A time interval measurement capability over a sufficient range to guarantee specified accuracy. The procedure requires the measurement of three arbitrary time intervals, in the low, middle, and high ends of the 5005A input range. Simultaneous measurements of each time interval are made by the 5005A and a high precision time interval counter. The two results are compared. The 5005A measurement should fall within the allowable tolerances.

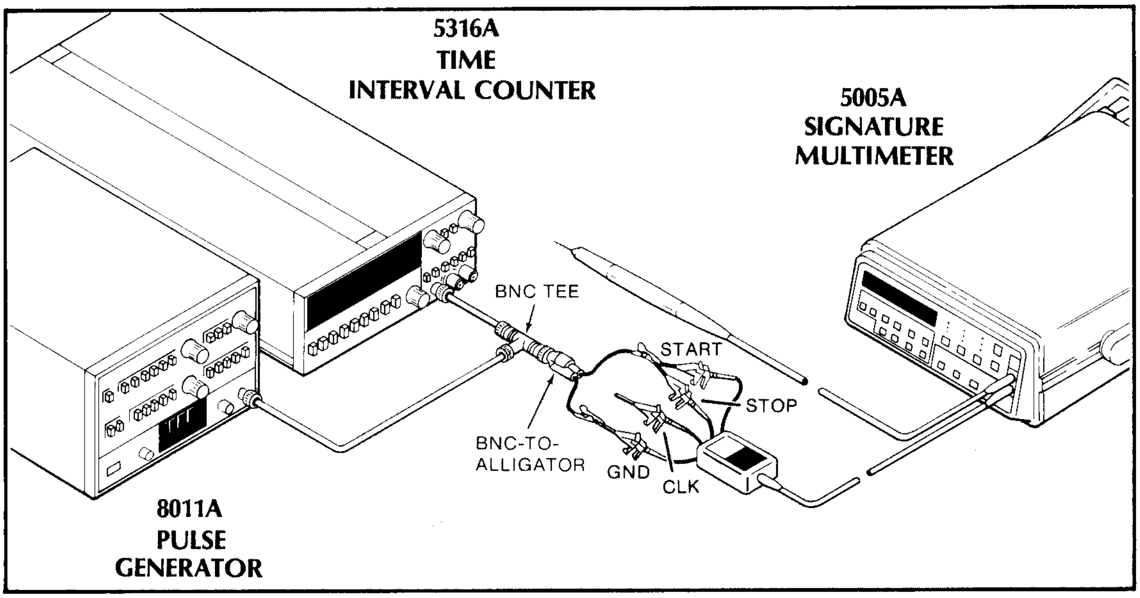

5316A
TIME
INTERVAL COUNTER
5005A
SIGNATURE
MULTIMETER
BNC TEE
START
STOP
BNC-TO-
ALLIGATOR
GND
CLK
8011A
PULSE
GENERATOR

Figure 4-17. Time Interval Reference Test Setup

Equipment:

Pulse Generator	8007B,8012A,8013B,8011A
Time Interval Counter	5316A

Optional Equipment:

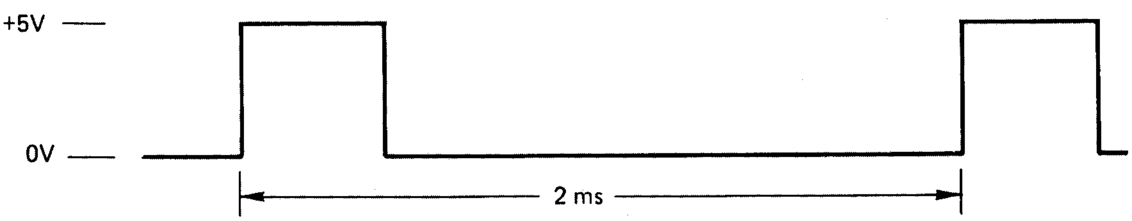
Logic Lab Breadboard	5035T

Procedure:

1. Set the pulse generator to output a 500 Hz waveform, five volts p-p, with a duty cycle as shown below. Verify the pulse width, using the high performance time interval counter.

NOTE

The 5316A is required only to accurately measure the pulse width. The pulse width can also be adjusted with an oscilloscope if necessary.


200 ns
+5V
0V
2 ms

2. Place the 5005A in the time interval mode (ms), with the Start Polarity set to _/¯ (pos) and the Stop Polarity set to ¯_ (neg).
3. Measure the time interval with the 5005A. The 5005A should display .0003 ±.0001 ms. Record the results on the Test Record.
4. Reconfigure the setup as shown in *Figure 4-18*. The remaining tests manually gate the time interval measurement, through simple switches on the Start and Stop inputs to logic low and high TTL Levels. If a 5316A is used, set controls as follows:

Function	TI A → B
Trig Levels/A and B	4.00 Volts
ATTN	X1
AC DC	DC
SEP/COM	SEP
SLOPE/A and B	_/¯

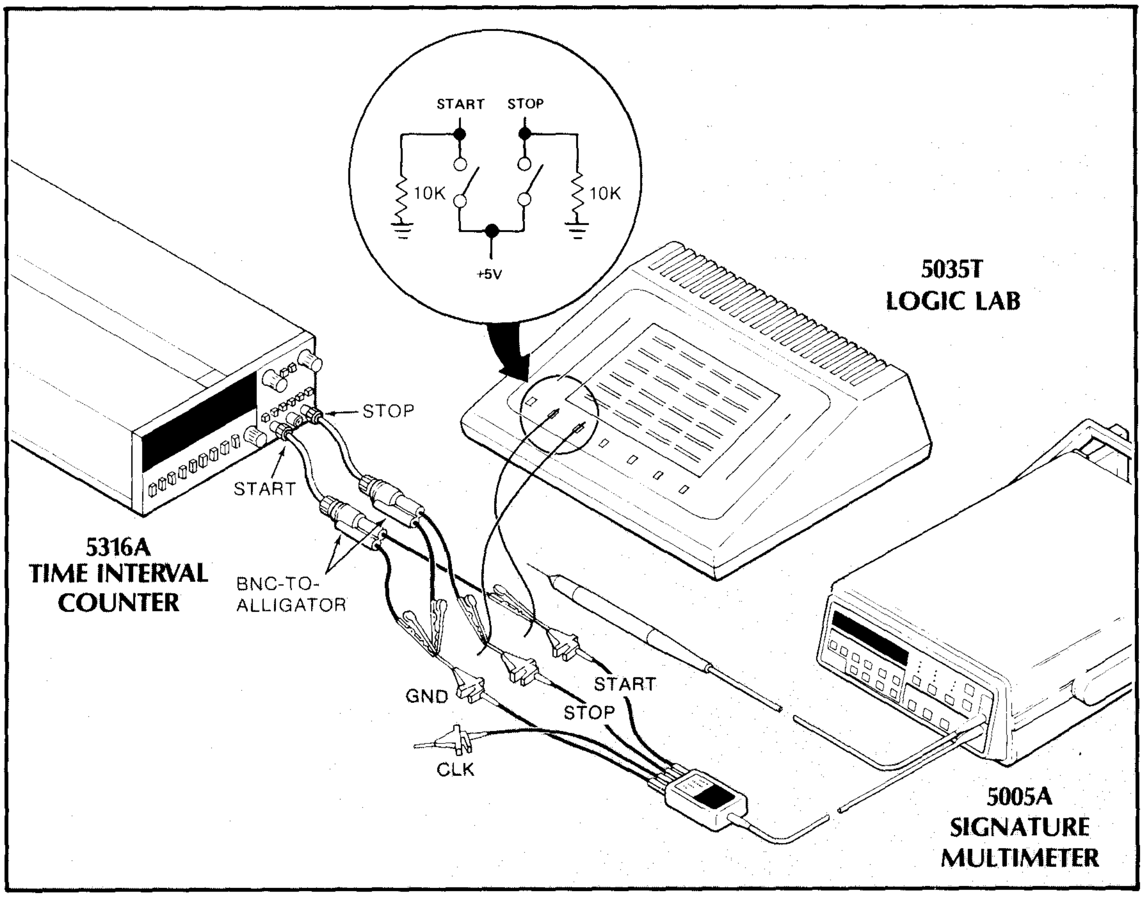

START
STOP
10K
10K
+5V
5035T
LOGIC LAB
STOP
START
5316A
TIME INTERVAL
COUNTER
BNC-TO-
ALLIGATOR
GND
START
STOP
CLK
5005A
SIGNATURE
MULTIMETER

Figure 4-18. Time Interval Test Setup II

5. Switch SW1 from Lo to Hi to Lo.
6. Switch SW2 from Lo to Hi to Lo.
7. The 5005A and the precision time interval counter should show approximately the same time interval. The time interval is determined by time between the switching of SW1 and SW2. The 5005A measurement should be within ±0.01% of the precision time interval counter measurement, ±1 count.

NOTE

The remaining steps require a Clock input.

8. Switch SW1 from Lo to Hi to Lo. Verify that the 5005A gate light is on.
9. After switching SW1, wait ≈60 seconds, then switch SW2 from Lo to Hi to Lo. Both counters should display ≈60 (seconds). The 5005A's maximum allowable error for 60 seconds is ±7 counts. Record the results in the Test Record.
10. Repeat steps 8 and 9, changing the wait (in step 9) to 90 seconds. The 5005A's maximum allowable error for 90 seconds is ±10 counts. Record the results in the Test Record.

4-28. DATA PROBE Performance Test (Setup and Hold)

Specification:

Setup Time	10 ns (data to be valid at least 10 ns before selected clock edge)
Hold Time	0 ns (data to be held until occurrence of selected clock edge)

Description: The following procedure is designed to test the setup (t_{DC}) and hold (t_{DH}) time constants within the 5005A Data Probe. Multiple pulse generators are configured to provide waveforms with adjustable duty cycles. The accuracy of the waveforms are monitored with a oscilloscope and time interval counter. The 5005A is set to the NORM Signature mode. The pulse waveform is varied for all combinations of 5005A data and clock controls. The t_{DC} or t_{DH}, displayed by the time interval counter, should remain within the given limits, and the 5005A signature should change as indicated.

NOTE

The specification for "t_{DC}" actually defines two conditions. The specification "t_{DC} minimum = 10 ns" for setup time means first; that the minimum or fastest allowable time between the data edge and the clock edge generated by the measurement timing source, cannot be less (or faster) than 10 ns. This is a conditional requirement for the unit from which signatures will be taken. Second, the t_{DC} minimum = 10 ns specification means that, given the first condition, the 5005A must now respond to the data and clock edges in less than 10 ns (max). Likewise, the t_{DH} specification for hold time (t_{DH}=0ns max) means the maximum time the 5005A needs to hold data before the occurance of the selected clock edge is "0 ns". During these tests, the frequency counter displays the t_{DC} and t_{DH} values for the test setups. The counter should display t_{DC} values less than 10 ns (typically 4 to 9 ns), and t_{DH} values less than 0 ns (typically -6 to 0 ns).

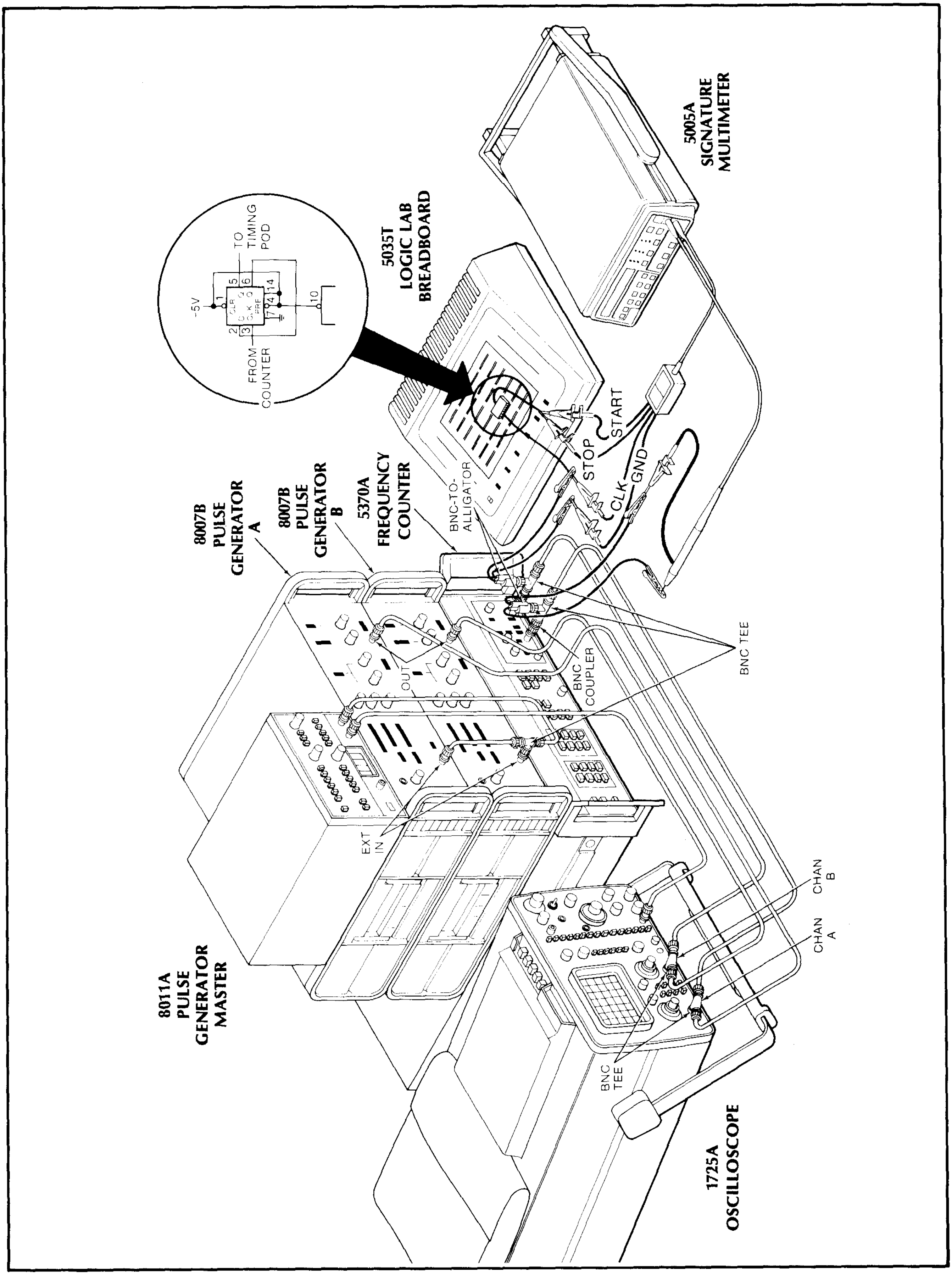

5005A
SIGNATURE
MULTIMETER
5035T
LOGIC LAB
BREADBOARD
-5V
1
5
6
14
2
3
7
4
10
CLR Q
CLK Q
PRE
FROM
COUNTER
TO
TIMING
POD
START
STOP
CLK
GND
BNC-TO-
ALLIGATOR
8007B
PULSE
GENERATOR
A
8007B
PULSE
GENERATOR
B
5370A
FREQUENCY
COUNTER
BNC TEE
BNC
COUPLER
OUT
EXT
IN
CHAN
B
CHAN
A
BNC
TEE
8011A
PULSE
GENERATOR
MASTER
1725A
OSCILLOSCOPE

Figure 4-19. Data Probe Test Setup

Equipment:

Pulse Generator	8011A
Pulse Generators (2)	8007A,8007B
Time Interval Counter	5370A
Oscilloscope	1725A
Divide by 2 network	74S74 IC

Optional Equipment:

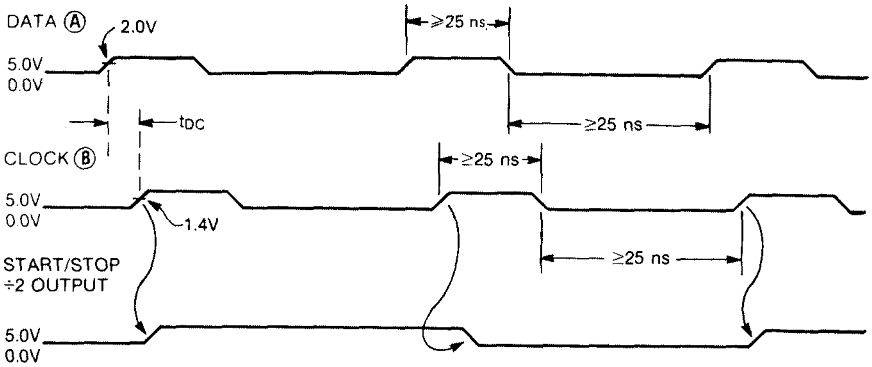
Logic Lab Breadboard	5035T

Procedure:

1. Set the master pulse generator to output a 20 MHz squarewave, at 5 volts p-p.
2. Using the delay and pulse width verniers of the two pulse generators (A and B), adjust the controls to produce the waveforms shown in *Figure 4-20.* The 5370A counter should be set to trigger at the prescribed levels as shown on the figures. Set the counter to the TI mode with Sample Size =1. The 5005A should be set to the NORM Signature Analysis mode with Start, Stop, and Clock controls as shown in the figures. Initially, with a t_{DC}=0ns, the 5005A should read 0000.
3. The t_{DC} delay can be changed by varying the pulse delay verniers of one of the pulse generators. The 5370A displays the value of tDC. Vary t_{DC} from 0 to 25 ns. The 5005A display should change from 0000 to 0001. This should occur with t_{DC} less than 10 ns. The point the change occurs at is the actual Data "1" rising edge clocked setup time. Typical times are from 4 to 9 ns. Record the results on the Test Record.
4. Repeat the procedure for the remaining three t_{DC} tests, changing the tested slope edges as indicated in *Figures 4-21* through *4-23.* Record the results on the Test Record.
5. The four data hold (t_{DH}) tests are analogous but the 5370A displays -t_{DH}. That is, when the counter displays -5 ns, record the absolute value, t_{DH} = 5 ns. Perform all four t_{DH} tests and verify that the t_{DH} specification (0 ns maximum) is met. Record the results on the Test Record.

NOTE

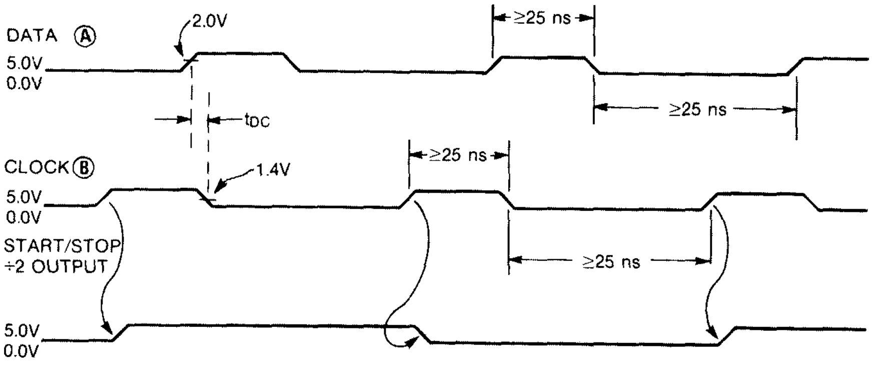
The following eight tests (Data Probe Setup Time, *Figures 4-20* through *4-23* and Data Probe Hold Time, *Figures 4-24* through *4-27*) all utilize the equipment setup shown in *Figure 4-19.* Each test, however, requires minor changes in control settings or procedure (e.g. change counter slope control from _/‾ to ‾_). As an aid to the technician, information shown in boldface type in *Figures 4-21* through *4-27,* highlight (only) the information which has changed from the previous test figure.


DATA Ⓐ
2.0V
5.0V
0.0V
≥25 ns
tDC
≥25 ns
CLOCK Ⓑ
≥25 ns
5.0V
0.0V
1.4V
START/STOP
÷2 OUTPUT
≥25 ns
5.0V
0.0V

DATA PROBE SETUP TIME

Setup		Method	Specifications
Waveform Edge	**Set 5005A Polarity to:**	Vary t_{DC} from 0 to 25 ns 5005A Display changes from 0000 to 0001	t_{DC} = 10 ns minimum
Ⓐ Data = Lo to Hi Ⓑ Clock = Rising Edge Set Counter Thresholds to: Data = A channel = 2.0V ╱ Clock = B channel = 1.4V ╱	START ☼ ● STOP ● ☼ CLOCK ☼ ●		

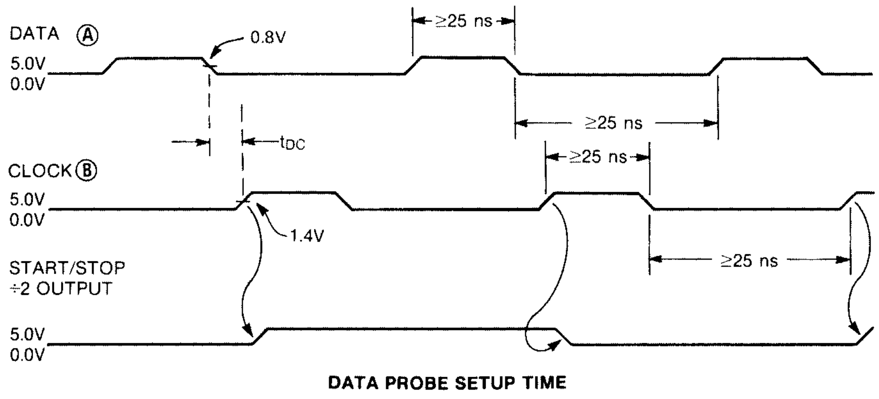
Figure 4-20. Data Probe Setup Time — Test 1


DATA Ⓐ
2.0V
5.0V
0.0V
≥25 ns
tDC
≥25 ns
CLOCK Ⓑ
1.4V
≥25 ns
5.0V
0.0V
START/STOP
÷2 OUTPUT
≥25 ns
5.0V
0.0V

DATA PROBE SETUP TIME

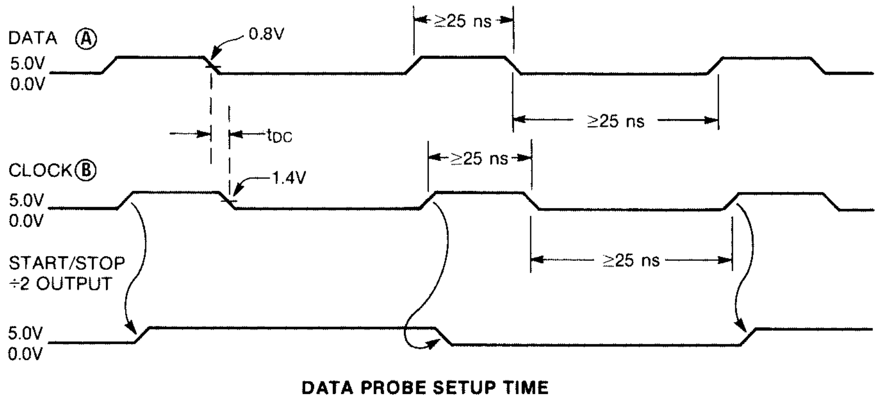
Setup		Method	Specifications
Waveform Edge	**Set 5005A Polarity to:**	Vary t_{DC} from 0 to 25 ns 5005A Display changes from 0000 to 0001	t_{DC} = 10 ns minimum
Ⓐ Data = Lo to Hi Ⓑ Clock = **Falling Edge** Set Counter Thresholds to: Data = A channel = 2.0V ╱ Clock = B channel = 1.4V ╲	START ☼ ● STOP ● ☼ **CLOCK** ● ☼		

Figure 4-21. Data Probe Setup Time — Test 2


DATA Ⓐ
5.0V
0.0V
0.8V
≥25 ns
≥25 ns
tDC
CLOCK Ⓑ
5.0V
0.0V
≥25 ns
1.4V
START/STOP
÷2 OUTPUT
≥25 ns
5.0V
0.0V
DATA PROBE SETUP TIME

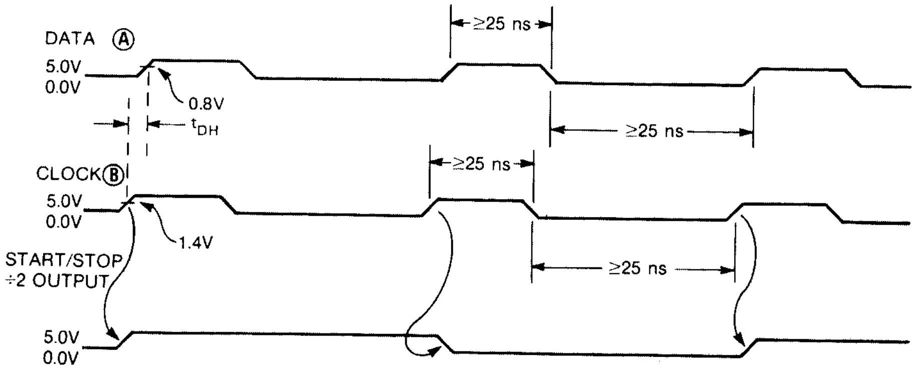
Setup		**Method**	**Specifications**
Waveform Edge	**Set 5005A Polarity to:**	Vary t_{DC} from 0 to 25 ns 5005A Display changes from **0001** to **0000**	t_{DC} = 10 ns minimum
Ⓐ Data = **Hi to Lo** Ⓑ Clock = **Rising Edge** Set Counter Thresholds to: Data = A channel = **0.8V** ↘ Clock = B channel = 1.4V ↗	START ☼ ● STOP ● ☼ **CLOCK** ☼ ●		

Figure 4-22. Data Probe Setup Time — Test 3


DATA Ⓐ
5.0V
0.0V
0.8V
≥25 ns
≥25 ns
tDC
CLOCK Ⓑ
1.4V
≥25 ns
5.0V
0.0V
START/STOP
÷2 OUTPUT
≥25 ns
5.0V
0.0V
DATA PROBE SETUP TIME

Setup		**Method**	**Specifications**
Waveform Edge	**Set 5005A Polarity to:**	Vary t_{DC} from 0 to 25 ns 5005A Display changes from 0001 to 0000	t_{DC} = 10 ns minimum
Ⓐ Data = Hi to Lo Ⓑ Clock = **Falling Edge** Set Counter Thresholds to: Data = A channel = 0.8V ↘ Clock = B channel = 1.4V ↘	START ☼ ● STOP ● ☼ **CLOCK** ● ☼		

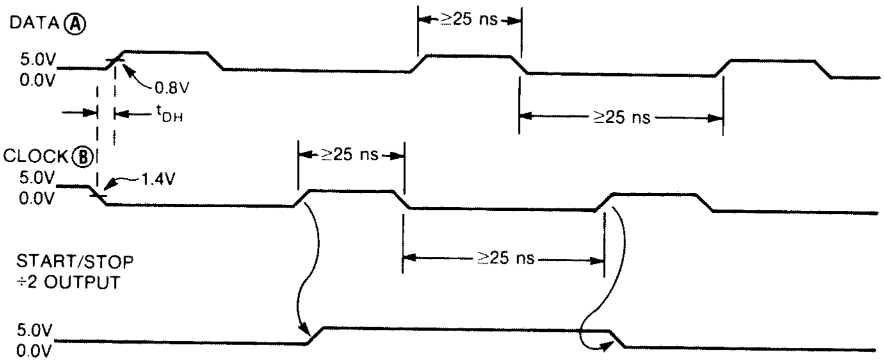
Figure 4-23. Data Probe Setup Time — Test 4


DATA Ⓐ
5.0V
0.0V
0.8V
t_{DH}
≥25 ns
≥25 ns
CLOCK Ⓑ
5.0V
0.0V
1.4V
≥25 ns
≥25 ns
START/STOP
÷2 OUTPUT
5.0V
0.0V

DATA HOLD TIME

Setup		Method	Specifications
Waveform Edge	**Set 5005A Polarity to:**		
Ⓐ Data = **Lo to Hi** Ⓑ Clock = **Rising Edge** Set Counter Thresholds to: Data = A channel = 0.8V ↗ Clock = B channel = 1.4V ↗	START ☼ ● STOP ● ☼ **CLOCK** ☼ ●	**Vary t_{DH} from +10 to −10 ns** 5005A Display changes from **0000** to **0001**	t_{DH} = 0 ns maximum
		Note: Counter displays $-t_{DH}$	

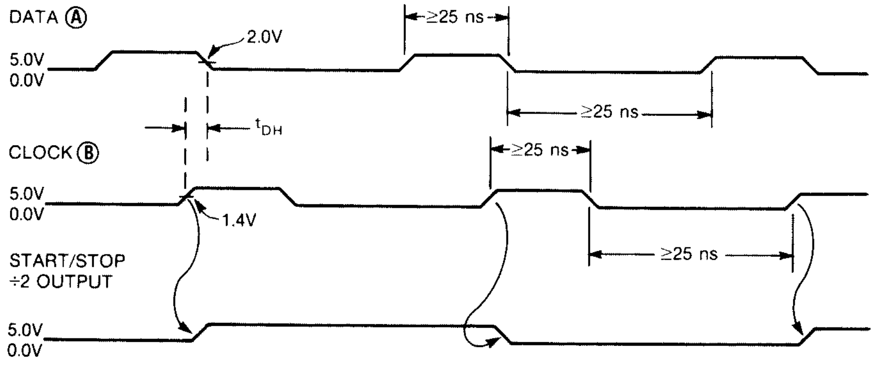
Figure 4-24. Data Hold Time — Test 1


DATA Ⓐ
5.0V
0.0V
0.8V
t_{DH}
≥25 ns
≥25 ns
CLOCK Ⓑ
5.0V
0.0V
1.4V
≥25 ns
≥25 ns
START/STOP
÷2 OUTPUT
5.0V
0.0V

DATA HOLD TIME

Setup		Method	Specifications
Waveform Edge	**Set 5005A Polarity to:**		
Ⓐ Data = Lo to Hi Ⓑ Clock = **Falling Edge** Set Counter Thresholds to: Data = A channel = 0.8V ↗ Clock = B channel = 1.4V ↘	START ☼ ● STOP ● ☼ **CLOCK** ● ☼	Vary t_{DH} from +10 to −10 ns 5005A Display changes from 0000 to 0001	t_{DH} = 0 ns maximum
		Note: Counter displays $-t_{DH}$	

Figure 4-25. Data Hold Time — Test 2


DATA Ⓐ
5.0V
0.0V
2.0V
≥25 ns
≥25 ns
t_{DH}
CLOCK Ⓑ
5.0V
0.0V
1.4V
≥25 ns
≥25 ns
START/STOP
÷2 OUTPUT
5.0V
0.0V

DATA HOLD TIME

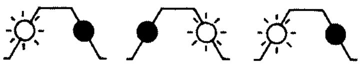
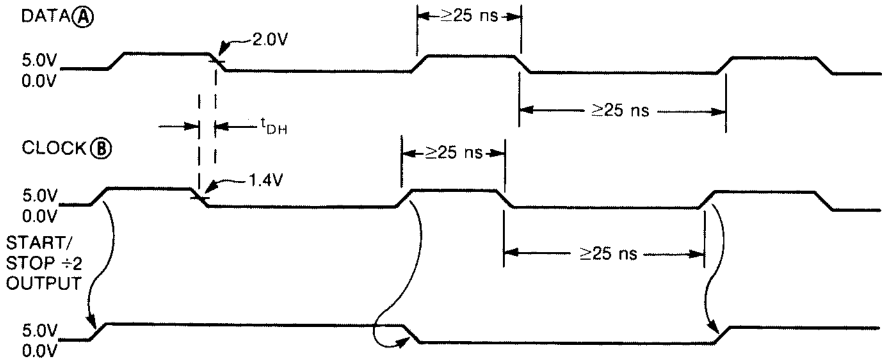
Setup		Method	Specifications
Waveform Edge	**Set 5005A Polarity to:**	Vary t_{DH} from +10 to −10 ns 5005A Display changes from **0001** to **0000**	t_{DH} = 0 ns maximum
Ⓐ Data = **Hi to Lo** Ⓑ Clock = **Rising Edge** Set Counter Thresholds to: Data = A channel = **2.0V** ╲ Clock = B channel = 1.4V ╱	START STOP **CLOCK** 	**Note**: Counter displays $-t_{DH}$	

Figure 4-26. Data Hold Time — Test 3


DATAⒶ
5.0V
0.0V
2.0V
≥25 ns
≥25 ns
t_{DH}
CLOCKⒷ
≥25 ns
1.4V
5.0V
0.0V
START/
STOP ÷2
OUTPUT
≥25 ns
5.0V
0.0V

DATA HOLD TIME

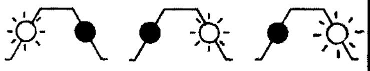
Setup		Method	Specifications
Waveform Edge	**Set 5005A Polarity to:**	Vary t_{DH} from +10 to −10 ns 5005A Display changes from 0001 to 0000	t_{DH} = 0 ns maximum
Ⓐ Data = Hi to Lo Ⓑ Clock = **Falling Edge** Set Counter Thresholds to: Data = A channel = 2.0V ╲ Clock = B channel = 1.4V ╲	START STOP **CLOCK** 	**Note**: Counter displays $-t_{DH}$	

Figure 4-27. Data Hold Time — Test 4

Table 4-2. Operation Verification Test Record

5005A S/N ____________ Date ____________

PARAGRAPH NO.	TEST	RESULTS
4-10	Self-Check	____________
4-11	Frequency Counter Test	____________
4-12	Totalizing Counter Test	____________
4-13	Time Interval Test	____________
4-14	Ohmmeter Test	____________
4-15	Voltmeter Test	____________
4-18	Normal Mode Test	____________
4-19	Qual Mode Test	____________

Table 4-3. Performance Test Record

Hewlett-Packard
Model 5005A
SIGNATURE MULTIMETER
Serial #

Tested by ______________________________

Date ______________________________

4-21. Resistance Perf Test

Resistor Range	Reference Measurement	Allowable Tolerance	HP 5005A Measurement
75 — 150 ohm	±1% ±2ΩW	________ to ________	________________
10 k — 20 k ohm	±1% ±2ΩW	________ to ________	________________
100 k — 200 k ohm	±1%	________ to ________	________________
500 k — 700 k ohm	±1%	________ to ________	________________
1.5 M — 2.0 M ohm	±1%	________ to ________	________________
4.0 M — 7.0 M ohm	±1%	________ to ________	________________

4-22. DC Voltage Perf Test

Source Voltage	Precision Voltmeter Measurement	Allowable Tolerance	HP 5005A DCV Measurement
-250.0V	________________	-250.7 to -249.3	________________
-27.00V	________________	-27.09 to -26.91	________________
-5.000V	________________	-5.007 to -4.993	________________
0.000V	________________	-0.002 to +0.002	________________
+5.000V	________________	+4.993 to +5.007	________________
+27.00V	________________	+26.91 to +27.09	________________
+250.0V	________________	+249.3 to 250.7	________________

4-23. Peak Voltage Perf Test

Peak Reference Level	Allowable Tolerance	HP 5005A Vp Measurement
(Positive Peak) +5.00V	+4.60 to +5.40	________________
(Negative Peak) -5.00V	-4.60 V to -5.40 V	________________

4-24. Differential Voltage Perf Test

Probe Tip Reference	dc Power Supply	Allowable Tolerance	5005A ΔD V Measurement
+250.0	+200.0	-49.855 to -50.145	________________
	+10.00	-239.380 to -240.620	________________
	-50.00	-299.230 to -300.770	________________
	-250.0	-498.730 to -501.270	________________

Probe Tip Reference	dc Power Supply	Allowable Tolerance	5005A ΔD V Measurement
-15.00	-20.00	-4.993 to -5.007	________________
	0.000	+14.983 to +15.017	________________
	+20.00	+34.963 to +35.037	________________
	-10.00	+4.993 to +5.007	________________

Table 4-3. Performance Test Record (Continued)

4-25. Frequency Perf Test

Source Frequency	Reference Measurement		5005A kHz Measurement
2 Hz		±1 count	
25 MHz		±4 counts	
50 MHz		±6 counts	

4-26. Totalizing Perf Test

of Pulses	Allowable Tolerance	5005A TOTLZ Measurement
0001	0000 to 0002	
50,000	49,999 to 50,001	
99,999	99,998 to 00000	

4-27. Time Interval Perf Test

Source Time Interval	Reference Measurement	Allowable Tolerance	HP 5005A Measurement
200 ns		to	
60 seconds		to	
90 seconds		to	

4-28. Data Probe Perf Test

Figure	Data	Clock	t_{DC}	t_{DH}	5005A Signature	Measurement
1	Lo to Hi	pos	10 ns Min		0000 → 0001	
2	Lo to Hi	neg	10 ns Min		0000 → 0001	
3	Hi to Lo	pos	10 ns Min		0001 → 0000	
4	Hi to Lo	neg	10 ns Min		0001 → 0000	
5	Lo to Hi	pos		0 ns Max	0000 → 0001	
6	Lo to Hi	neg		0 ns Max	0000 → 0001	
7	Hi to Lo	pos		0 ns Max	0001 → 0000	
8	Hi to Lo	neg		0 ns Max	0001 → 0000	

SECTION V

ADJUSTMENTS

5-1. INTRODUCTION

5-2. This section describes the adjustments which will return the 5005A to peak operating condition after repairs are completed. If the adjustments are to be considered valid, the 5005A line voltage must be within +5% to -10% of nominal.

5-3. In general, periodic adjustment should not be necessary. However, to assure proper calibration, it is recommended that these adjustments be performed whenever repairs are made or the instrument fails the Performance Verification procedures in Section IV. The adjustment procedures in *Table* 5-1 are listed in numeric order according to the assembly number. The order of adjustment is not critical, the procedures are in numeric order only for quick and easy reference.

5-4. SAFETY CONSIDERATIONS

5-5. Although the 5005A has been designed in accordance with international safety standards, this manual contains information, cautions, and warnings which MUST be followed to ensure safe operation and to retain the 5005A in safe condition (also see Section VIII of this manual). Service and adjustments should be performed only by qualified personnel.

WARNING

ANY INTERRUPTION OF THE PROTECTIVE (GROUNDING) CONDUCTOR OR DISCONNECTION OF THE PROTECTIVE EARTH TERMINAL IS LIKELY TO MAKE THE 5005A DANGEROUS.

CAUTION

The A2 DVM Printed Circuit Board is a high impedance pc board. It is extremely sensitive to contamination from dirt and oils, applied when handling with bare hands. Contamination can cause nonlinearity, drift, or inoperation. Do not handle the A2 DVM assembly with bare fingers, except at the edges. Refer to Paragraph 8-56 for proper handling and cleaning procedures.

5-6. Any adjustment, maintenance, or repair of the opened 5005A with voltage applied should be avoided as much as possible, and when inevitable should be carried out by a skilled person who is aware of the hazard involved. Capacitors inside the 5005A may still be charged even if the 5005A has been disconnected from its source of supply.

5-7. Make sure that only fuses with the required rated current and of the specified type are used for replacement. The use of repaired fuses and the short circuiting of fuseholders must be avoided. Whenever it is likely that the protection offered by fuses has been impaired, the 5005A must be rendered inoperative and secured against any operation until repaired.

WARNING

ADJUSTMENTS DESCRIBED HEREIN ARE PERFORMED WITH POWER SUPPLIED TO THE 5005A WHILE THE PROTECTIVE COVERS ARE REMOVED. ENERGY AVAILABLE AT THE REAR PANEL LINE MODULE MAY, IF CONTACTED, RESULT IN PERSONAL INJURY.

5-8. EQUIPMENT REQUIRED

5-9. The test equipment required for the adjustments is listed in *Table 1-2,* Recommended Test Equipment. The critical specifications of any substitute test equipment must meet or exceed the standards listed in *Table 1-2* if the 5005A is to meet the specifications in *Table 1-1.*

5-10. ADJUSTMENT LOCATIONS

5-11. As an adjustment aid, *Figures 5-1* and *5-8* are provided to quickly locate and identify adjustment points in the instrument. These photos show variable resistors, variable capacitors, test points, etc., needed for adjustment of the instrument.

Table 5-1. Adjustments

Procedure	Assembly	Adjustment	Comments
Input Compensation Adjustments	A1	C5	Data Probe Input
	A1	C6	Start/ST-SP Input
	A1	C7	Stop/Qual Input
	A1	C8	Clock Input
Precision Reference Voltage Adjustment	A2	R2	Set for +10.000 Vdc

5-12. ADJUSTMENT PROCEDURES

5-13. INPUT COMPENSATION ADJUSTMENTS

5-14. The following procedures are provided to fine tune the high frequency compensation circuits for the Data Probe and Pod inputs. The input circuitry is adjusted for minimum waveform distortion into each respective input comparator. This is accomplished by applying a squarewave to each input and monitoring the corresponding comparator output. The comparator output is observed using an oscilloscope, while varying the dc offset of the input signal. If the input circuitry is adjusted to under compensate, the rising edge of the waveform into the comparator will be slower, and any change in the dc offset of the input will affect the timing at the leading edge of the comparator output pulse. If the input circuitry is adjusted to over compensate, the waveform at the comparator input will have an overshoot. At some dc offset value, the output pulse of the comparator will occur only for the duration of the overshoot, with the trailing edge timing dependant on the dc offset. In a properly compensated circuit, the dc offset of the input signal can cause the appearance or disappearance of the pulse at the comparator output, but will not affect its width.

5-15. The input compensation adjustment is made to produce minimum distortion in the leading and trailing edges of extremely fast input signals. It is important to use an input pulse generator with very fast transition times, typically 2ns or better.

5-16. The following procedures will adjust each of the four inputs to the 5005A (Data Probe, ST-SP/START, QUAL/STOP, and CLOCK) such that each respective comparator output pulse appears and disappears cleanly, with no change in pulse width, as the input signal dc offset is varied.

5-17. Preliminary Adjustment Procedure.

5-18. To perform the input compensation adjustments, access and locate the adjustments on the A1 Main Assembly, by refering to *Figure 5-1*. Assemble and preset the test equipment as follows:

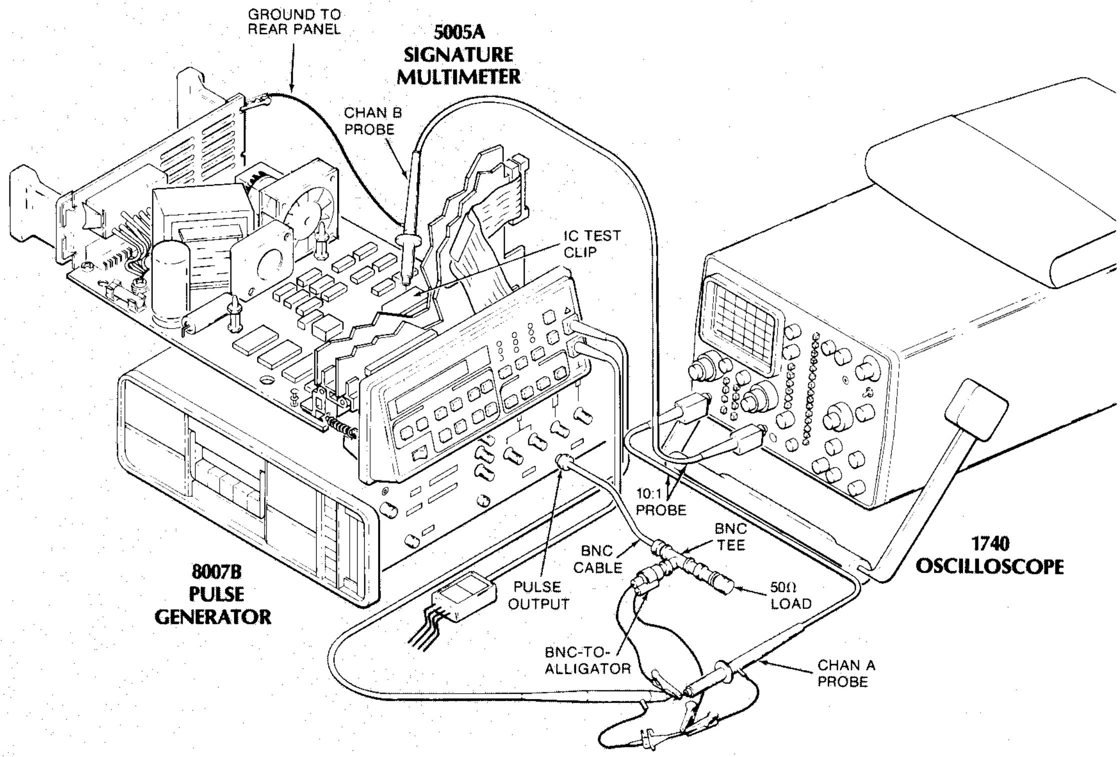
a. Refer to the disassembly procedures in Section VIII and remove the 5005A top cover and handle. Remove the complete instrument from the bottom cover. Holding it in a horizontal position, rotate the instrument 90 degrees (clockwise) and rest it on the bottom cover.

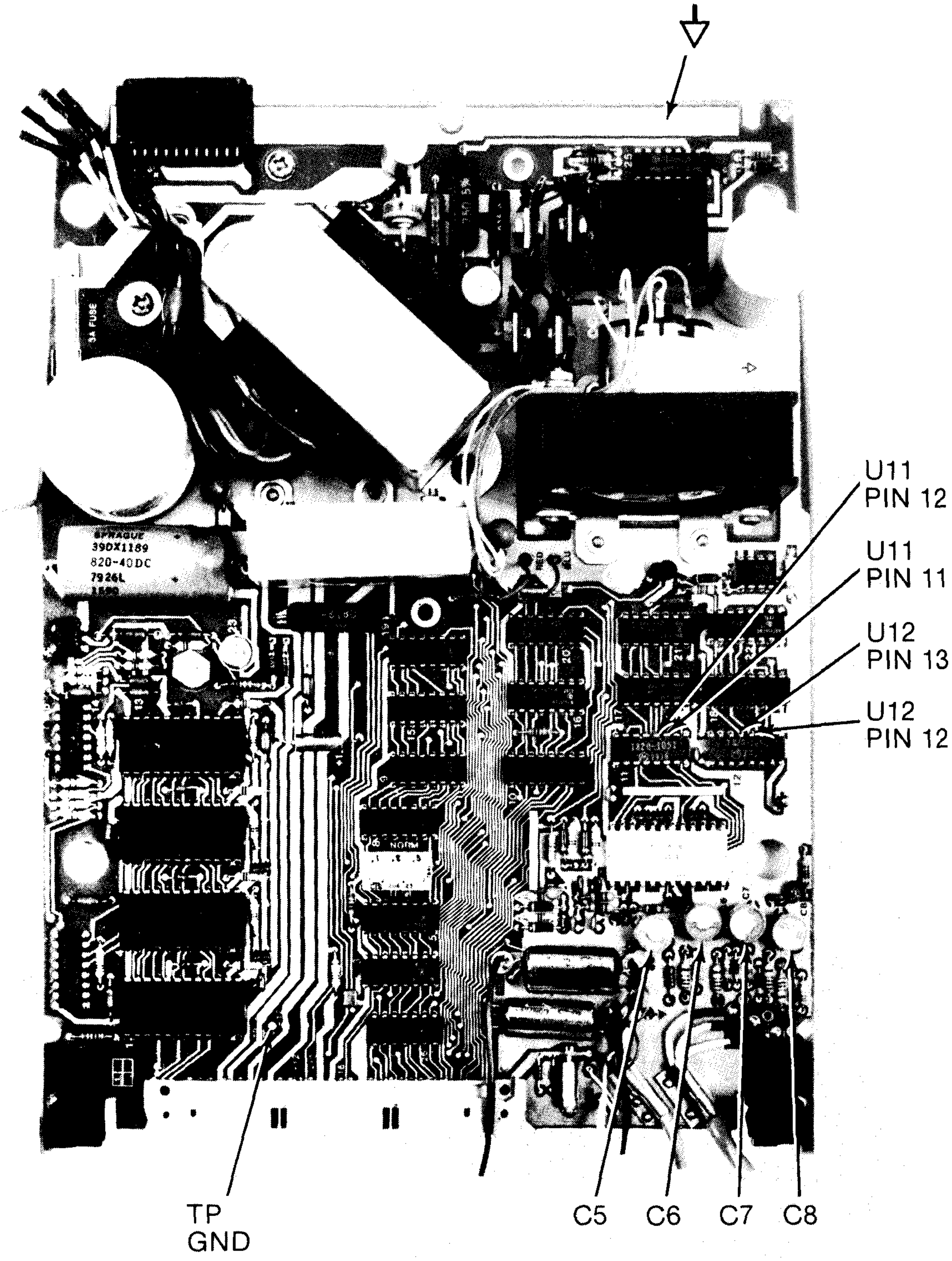
CAUTION

The A2 DVM Printed Circuit Board is a high impedance pc board. It is extremely sensitive to contamination from dirt and oils, applied when handling with bare hands. Contamination can cause nonlinearity, drift, or inoperation. Do not handle the A2 DVM assembly with bare fingers, except at the edges.

b. The top two printed circuit assemblies, A2 DVM Assy and A3 Microprocessor Assy, are hinged for ease of service. Refering to the disassembly procedures in Section VIII, remove the retaining springs and carefully slide the front panel assembly forward. Raise the A2 DVM and A3 Microprocessor assemblies on their hinges, allowing access to the adjustments and test points on A1 Main Assy.

c. Set up the equipment as follows:


GROUND TO REAR PANEL
5005A SIGNATURE MULTIMETER
CHAN B PROBE
IC TEST CLIP
10:1 PROBE
BNC TEE
BNC CABLE
50Ω LOAD
1740 OSCILLOSCOPE
8007B PULSE GENERATOR
PULSE OUTPUT
BNC-TO-ALLIGATOR
CHAN A PROBE


U11
PIN 12
U11
PIN 11
U12
PIN 13
U12
PIN 12
TP
GND
C5
C6
C7
C8
SPRAGUE
39DX1189
820-40DC
7926L

A1 MAIN ASSEMBLY

Figure 5-1. Input Compensation Adjustments

d. Set the HP 1740A controls as follows:

CHANNEL A	DC Coupled, .02 Volts/Div
CHANNEL B	DC Coupled, .2 Volts/Div
SWEEP	AUTO
VERTICAL DISPLAY	ALT
HORIZONTAL DISPLAY	MAIN
INT TRIGGER	A
TIME/DIV	.2 mSEC

e. Set the pulse generator to output a squarewave, ≈500 mv p-p, at a 1 kHZ rate. Adjust the leading and trailing edge controls for the fastest possible transition times, i.e. the squarest squarewave. Set the pulse generator output dc offset to the adjustable mode. See *Figure 5-2.* If an HP 8007B is available, set the controls as follows:

RATE	.3K-10K
RATE VERNIER	Adjust for 1 KHz
PULSE DELAY	5 n - 50 n (DELAY)
PULSE DELAY VERNIER	Fully CCW
PULSE WIDTH	50 µ - 1.5 m (Sec)
PULSE WIDTH VERNIER	Adjust for 50-50 Duty Cycle
TRIGGER MODE	NORM
TRANSITION TIME	2.0 n - 0.1µ (Sec)
LEADING EDGE	Fully CCW
TRAILING EDGE	Fully CCW
AMPLITUDE	0.5-1.0 (V)
AMPLITUDE VERNIER	Adjust for 500 mv/p-p
OFFSET	ON
OFFSET VERNIER	Per Adjustment

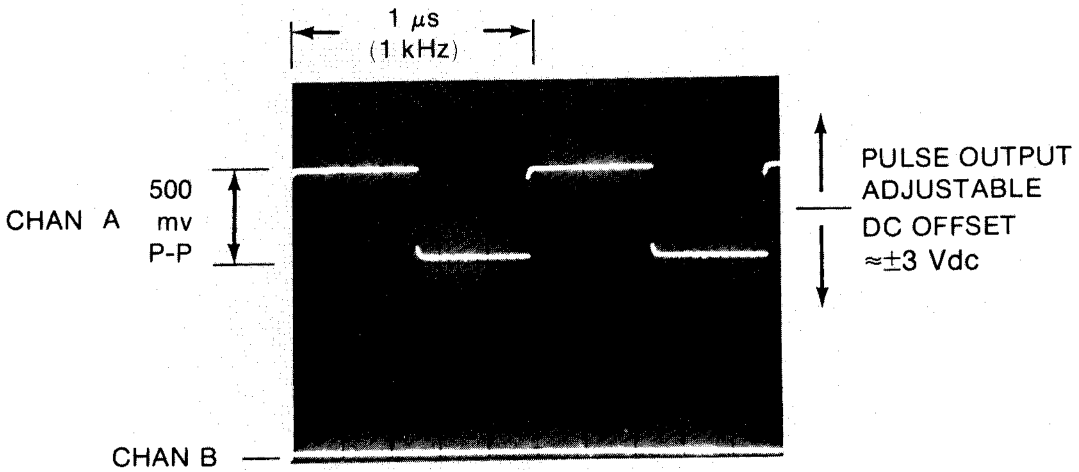


Figure 5-2. Pulse Generator Output

f. Set the HP 5005A controls as follows:

LINE	ON
SIGNATURE	NORM
THRESHOLDS	TTL

5-19. Input Compensation Adjustment Procedures (A1 Motherboard Assy)

Input	Adjust	Connect Point
Data Probe	C5	A1 U12, pin 12
ST-SP/Start	C6	A1 U11, pin 12
Stop/Qual	C7	A1 U11, pin 13
Clock	C8	A1 U12, pin 13

a. Connect the Channel A oscilloscope probe to the pulse generator PULSE OUTPUT as shown in the set-up diagram.

b. Connect the Channel B oscilloscope probe to A1 U12, pin 12, and connect the ground clip to the 5005A rear panel.

c. Connect the 5005A Data Probe tip to the pulse generator PULSE OUTPUT. Connect the Data Probe ground wire to the closest ground connection.

d. Begin with the Pulse Generator OFFSET VERNIER set to the fully positive offset position. Using the OFFSET VERNIER, slowly lower the dc offset of the input signal until the comparator output on the oscilloscope Channel B "just" begins to trigger. This is indicated by a likeness of the input squarewave on the oscilloscope Channel A, appearing on Channel B. The Channel A POSN control should be readjusted as necessary, to return the input waveform to the oscilloscope display. Readjust the OFFSET VERNIER slightly positive until the comparator output, on Channel B, intermittently triggers, displaying trailing edge jitter as shown in *Figure 5-3*.

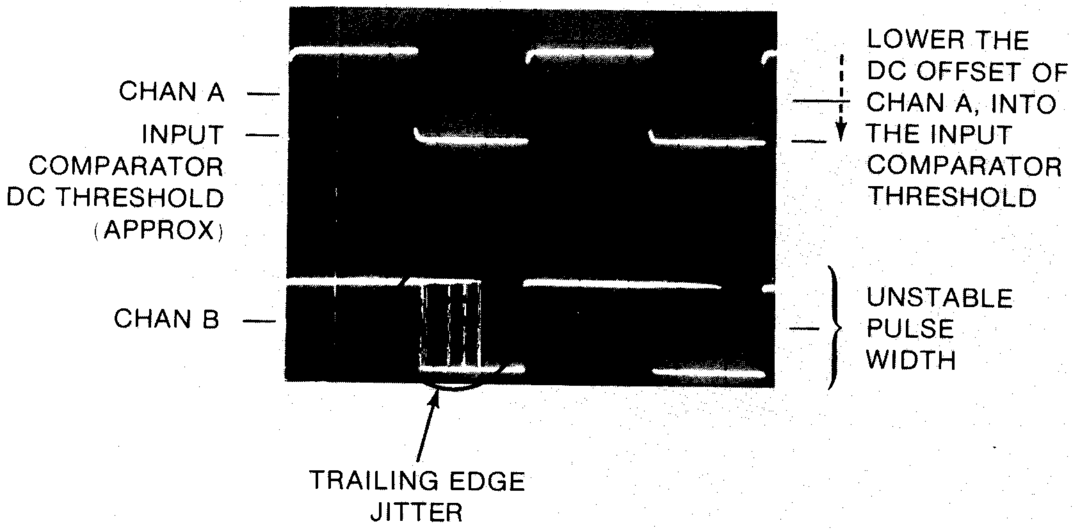

CHAN A
INPUT COMPARATOR DC THRESHOLD (APPROX)
CHAN B
LOWER THE DC OFFSET OF CHAN A, INTO THE INPUT COMPARATOR THRESHOLD
UNSTABLE PULSE WIDTH
TRAILING EDGE JITTER

Figure 5-3. Under Compensated

e. Using a non-metallic screwdriver adjust A1 C5 for a stable, symmetrical squarewave. Readjust the OFFSET VERNIER slightly positive again, until the trailing edge jitter reappears. Readjust A1 C5. Repeat this routine until the capacitor (C5) is adjusted such that the comparator output on Channel B "snaps-in", displaying a stable symmetrical squarewave as early as possible, while varying the input OFFSET VERNIER. When properly adjusted, the Channel B display may be intermittent, but the pulse width should not vary. That is, the comparator may be triggering at times, and not triggering at other times, producing an unstable display (see *Figure 5-4*), but there should be no trailing edge jitter and the pulse width should never be less than the 50-50 duty cycle shown in *Figure 5-5*.

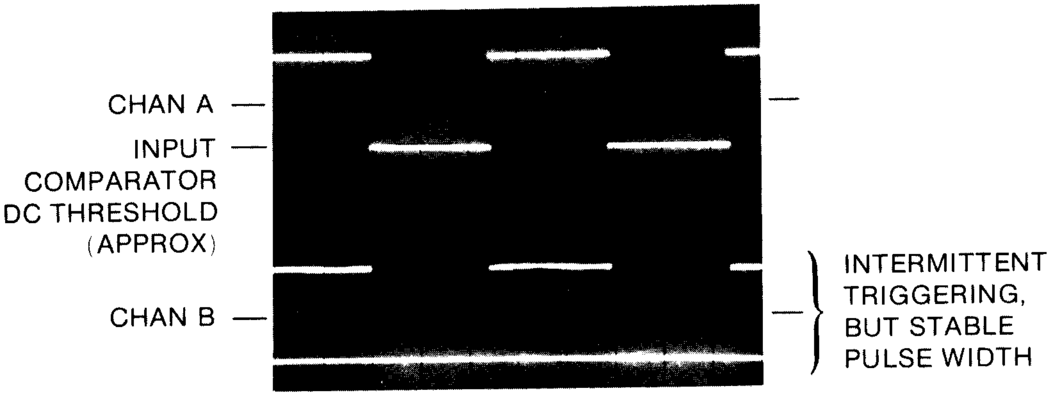

CHAN A
INPUT COMPARATOR DC THRESHOLD (APPROX)
CHAN B
INTERMITTENT TRIGGERING, BUT STABLE PULSE WIDTH

Figure 5-4. Proper Compensation (Intermittent)

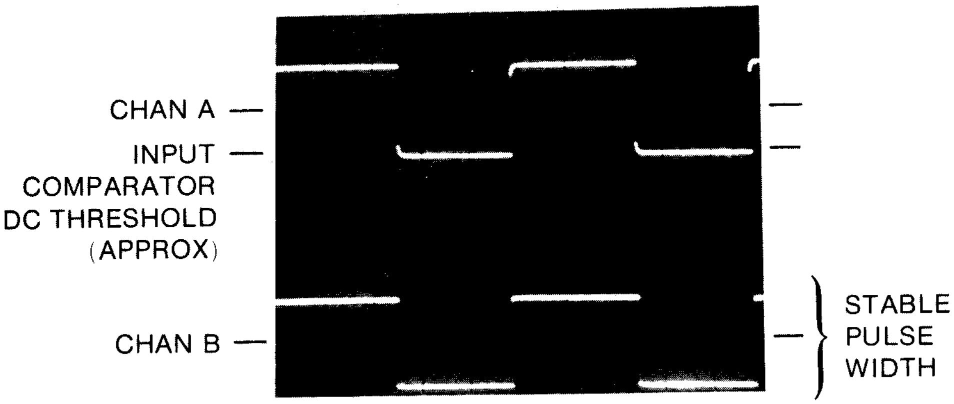

CHAN A
INPUT COMPARATOR DC THRESHOLD (APPROX)
CHAN B
STABLE PULSE WIDTH

Figure 5-5. Proper Compensation (Stable)

f. Repeat the procedures in steps d. and e., with the OFFSET VERNIER set to the fully negative position. Ensure that the comparator output snaps in cleanly, with no leading edge jitter, as the dc offset of the input signal is raised into the comparator threshold. Refer to *Figures 5-6* and *5-7*.

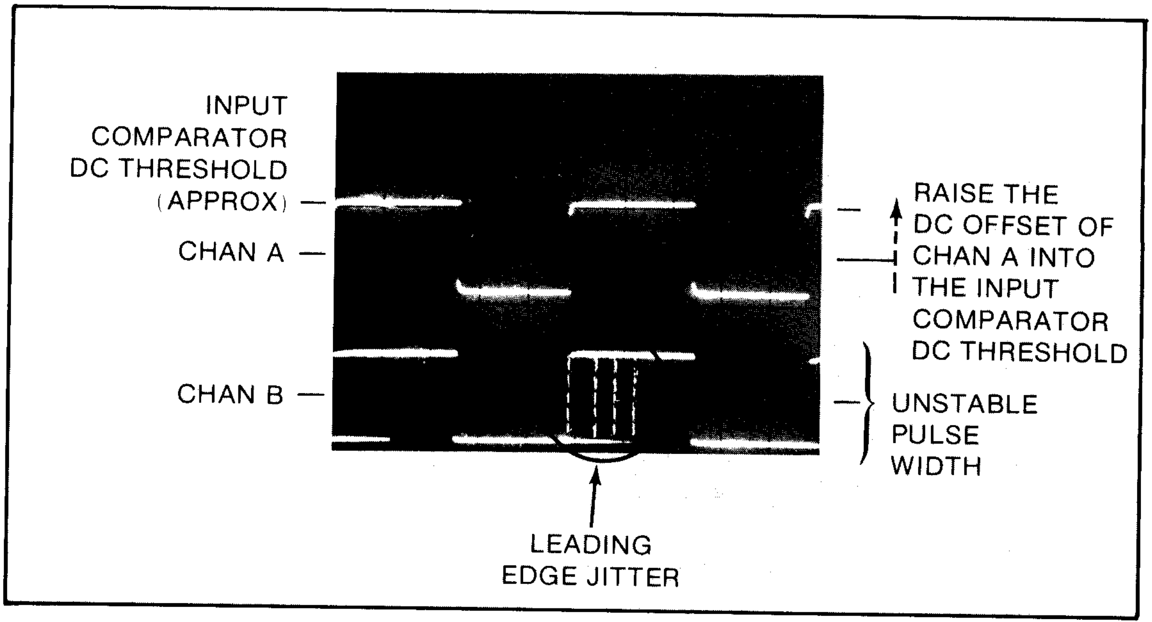

INPUT COMPARATOR DC THRESHOLD (APPROX)
CHAN A
CHAN B
RAISE THE DC OFFSET OF CHAN A INTO THE INPUT COMPARATOR DC THRESHOLD
UNSTABLE PULSE WIDTH
LEADING EDGE JITTER

Figure 5-6. Over Compensated

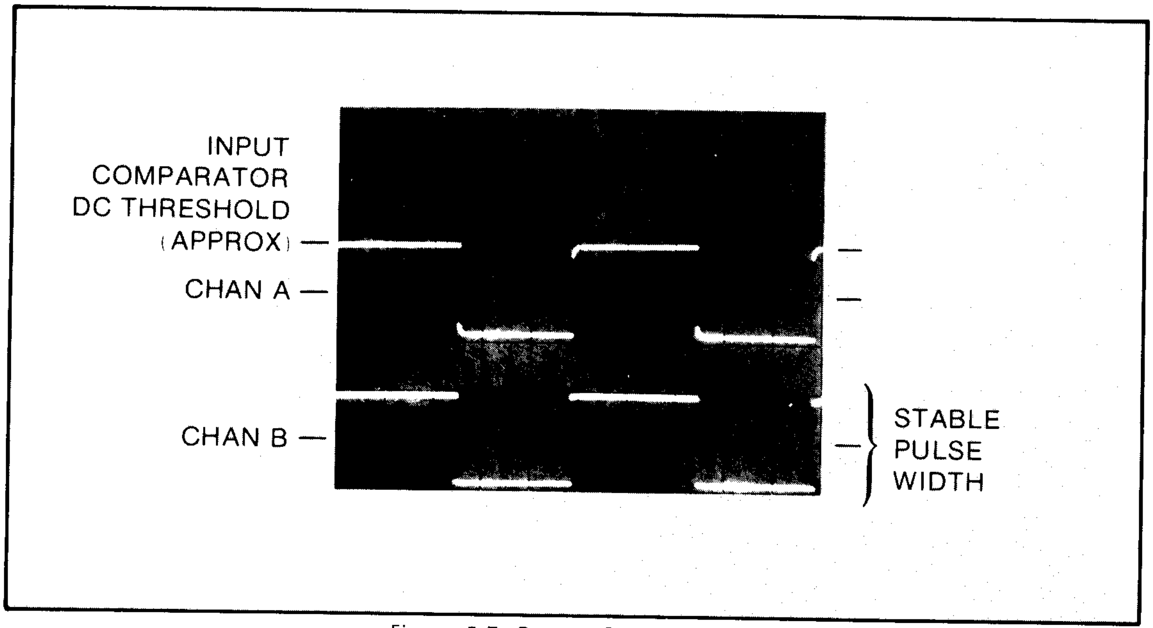

INPUT COMPARATOR DC THRESHOLD (APPROX)
CHAN A
CHAN B
STABLE PULSE WIDTH

Figure 5-7. Proper Compensation

g. Disconnect the Data Probe and the Channel B oscilloscope probe.

h. Connect the Channel B oscilloscope probe to A1 U11, pin 12, and connect the ground clip to the 5005A rear panel.

i. Connect the 5005A Pod START/ST-SP connector to the pulse generator PULSE OUTPUT. Connect the Pod ground (⊥) connector to the closest ground connection.

j. Repeat the procedures in steps d. through f., substituting C6 for C5.

k. Disconnect the 5005A Pod START/ST-SP connector.

l. Connect the Channel B oscilloscope probe to A1 U11, pin 13, and connect the ground clip to the 5005A rear panel.

m. Connect the 5005A Pod STOP/QUAL connector to the pulse generator PULSE OUTPUT. Connect the Pod ground (⊥) connector to the closest ground connection.

n. Repeat the procedures in steps d. through f., substituting C7 for C5.

o. Disconnect the 5005A Pod STOP/QUAL connector.

p. Connect the Channel B oscilloscope probe to A1 U12, pin 13, and connect the ground clip to the 5005A rear panel.

q. Connect the 5005A Pod CLOCK connector to the pulse generator PULSE OUTPUT. Connect the Pod ground (⊥) connector to the closest ground connection.

r. Repeat the procedures in steps d. through f., substituting C8 for C5.

s. This completes the input compensation adjustments.

5-20. Precision Reference Voltage Adjustment (A2 DVM Assy)

5-21. The following procedure adjusts and verifies the +10.00Vdc precision reference voltage, on the A2 DVM assembly. The only test equipment required is a Digital Voltmeter. Refer to *Table 1-2*, for the minimum specification requirements for test equipment.

CAUTION

The A2 DVM Printed Circuit Board is a high impedance pc board. It is extremely sensitive to contamination from dirt and oils, applied when handling with bare hands. Contamination can cause nonlinearity, drift, or inoperation. Do not handle the A2 DVM assembly with bare fingers, except at the edges. Refer to Paragraph 8-56 for proper handling and cleaning procedures.

5-22. To perform the +10.00V Precision Reference adjustment, refer to *Figure 5-8*, access and locate the adjustment and test points on the A2 DVM assembly. Assemble and preset the test equipment as follows:

a. Refer to the disassembly procedures in Section VIII and remove the 5005A top cover and handle. Remove the complete instrument from the bottom cover. Holding it in a horizontal position, rotate the instrument 90 degrees (clockwise) and rest it on the bottom cover.

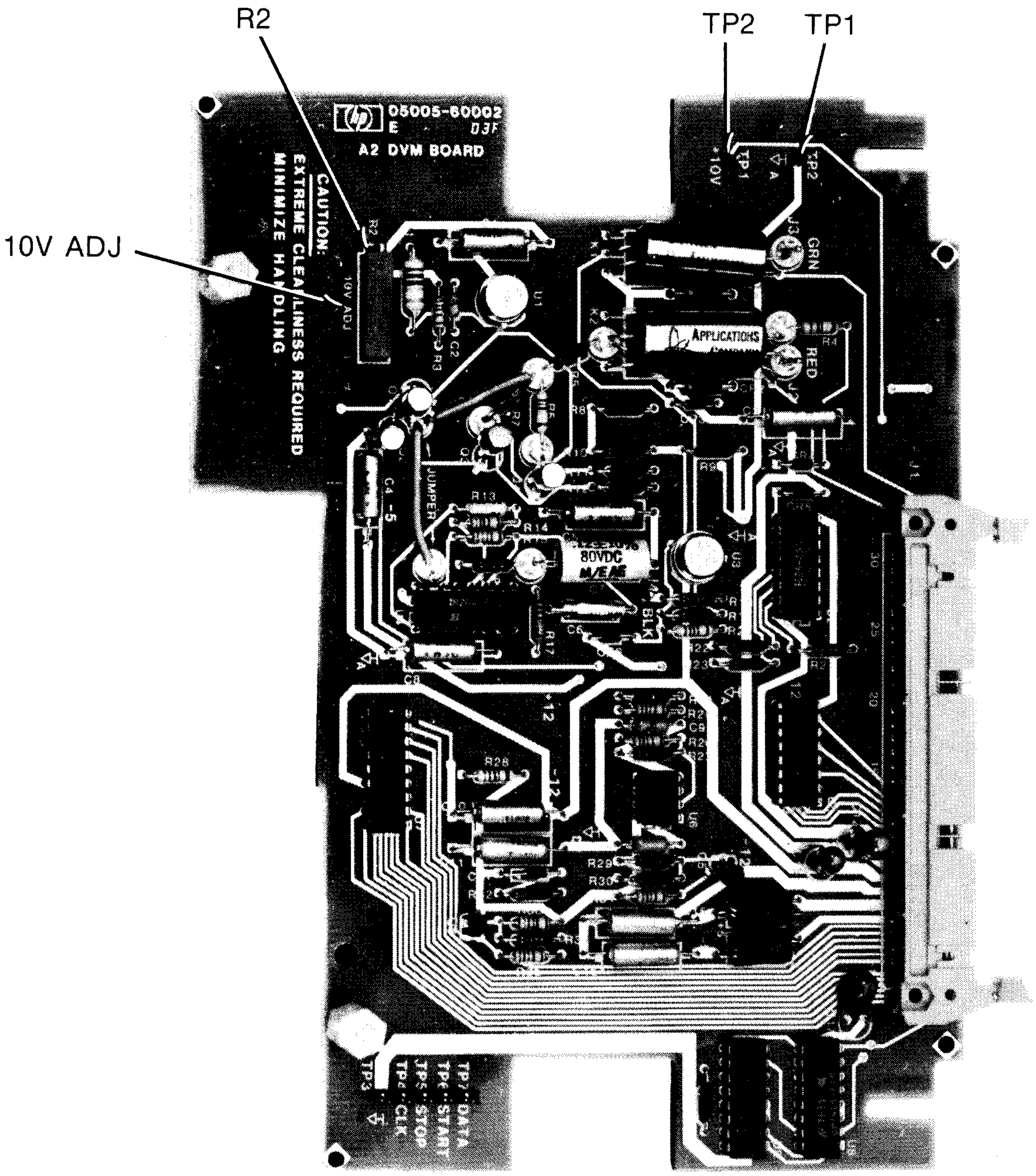
b. The top two printed circuit assemblies, A2 DVM Assy and A3 Microprocessor Assy, are hinged for ease of serviceability. Referring to the disassembly procedures in Section VIII, remove the retaining springs and carefully slide the front panel assembly forward. Raise the A3 assembly on its hinges allowing access to the adjustment and test points on A2 DVM Assembly.

c. Connect the DVM positive lead to A2 DVM Assy TP1 (+10V), and negative lead to A2 TP2 (ground).

d. Set 5005A LINE switch to ON.

e. Adjust A2 R2 for a reading of +10.000 ± .001V.

f. Disconnect all test equipment. This completes the adjustment of the Precision Reference Voltage.


R2
TP2
TP1
10V ADJ
05005-60002
A2 DVM BOARD
CAUTION:
EXTREME CLEANLINESS REQUIRED
MINIMIZE HANDLING
TP7 DATA
TP6 START
TP5 STOP
TP4 CLK
TP3

A2 DVM ASSEMBLY

Figure 5-8. +10.00V Precision Reference Adjustment

SECTION VI
REPLACEABLE PARTS

6-1. INTRODUCTION

6-2. This section contains information for ordering parts. *Table 6-1* lists abbreviations used in the parts list and throughout the manual. *Table 6-2* lists all replaceable parts in reference designation order. *Table 6-3* contains the names and addresses that correspond with the manufacturer's code numbers.

6-3. ABBREVIATIONS

6-4. *Table 6-1* lists abbreviations used in the parts list, and throughout the manual. In some cases, two forms of the abbreviations are used, one all in capital letters, and one partial or no capitals. This occurs because the abbreviations in the parts list are always all capitals. However, in the schematics and other parts of the manual, other abbreviation forms are used with both lower case and upper case letters.

6-5. REPLACEABLE PARTS LIST

6-6. *Table 6-2* is the list of replaceable parts and is organized as follows:

a. Electrical assemblies and their components in alphanumerical order by reference designation.

b. Chassis-mounted parts in alphanumerical order by reference designation.

c. Miscellaneous parts.

6-7. The information given for each part consists of the following:

a. The Hewlett-Packard part number.

b. Part number check digit (CD).

c. The total quantity (Qty) in the assembly.

d. The description of the part.

e. A typical manufacturer of the part in a five-digit code.

f. The manufacturer's number of the part.

6-8. The total quantity for each part is given only once — at the first appearance of the part number in the list.

6-9. MANUFACTURERS CODE LIST

6-10. *Table 6-3* contains the names and addresses that correspond to the manufacturer's code numbers.

6-11. ORDERING INFORMATION

6-12. To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number, the check digit, indicate the quantity required, and address the order to the nearest Hewlett-Packard office. The check digit will ensure accurate and timely processing of your order.

6-13. To order a part that is not listed in the replaceable parts table, include the instrument model number, instrument serial number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard Office.

6-14. DIRECT MAIL ORDER SYSTEM

6-15. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

a. Direct ordering and shipment from the HP Parts Center in Mountain View, California.

b. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local HP office when the orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices — to provide these advantages, a check or money order must accompany each order.

6-16. Mail order forms and specific ordering information is available through your HP office. Addresses and phone numbers are located at the back of this manual.

6-17. CABINET PARTS AND HARDWARE

6-18. To locate and identify miscellaneous cabinet parts and instrument hardware, refer to *Figures 6-1* through *6-5*. These figures provide various exploded views of the instrument, identified with Reference Designators. A table is provided opposite each illustration, containing part number, description, and quantity information for each reference designator shown. The quantity indicated represents the total number used within the instrument.

Table 6-1. Reference Designations and Abbreviations

REFERENCE DESIGNATIONS

A = assembly
AT = attenuator; isolator; termination
B = fan; motor
BT = battery
C = capacitor
CP = coupler
CR = diode; diode thyristor; varactor
DC = directional coupler
DL = delay line
DS = annunciator; signaling device (audible or visual); lamp; LED
E = miscellaneous electrical part
F = fuse
FL = filter
H = hardware
HY = circulator
J = electrical connector (stationary portion); jack
K = relay
L = coil; inductor
M = metre
MP = miscellaneous mechanical part
P = electrical connector (movable portion); plug
Q = transistor; SCR; triode thyristor
R = resistor
RT = thermistor
S = switch
T = transformer
TB = terminal board
TC = thermocouple
TP = test point
U = integrated circuit; microcircuit
V = electron tube
VR = voltage regulator; breakdown diode
W = cable; transmission path; wire
X = socket
Y = crystal unit-piezo-electric
Z = tuned cavity; tuned circuit

ABBREVIATIONS

A = ampere
ac = alternating current
ACCESS = accessory
ADJ = adjustment
A/D = analog-to-digital
AF = audio frequency
AFC = automatic frequency control
AGC = automatic gain control
AL = aluminum
ALC = automatic level control
AM = amplitude modulation
AMPL = amplifier
APC = automatic phase control
ASSY = assembly
AUX = auxiliary
AVG = average
AWG = american wire gauge
BAL = balance
BCD = binary coded decimal
BD = board
BE CU = beryllium copper
BFO = beat frequency oscillator
BH = binder head
BKDN = breakdown
BP = bandpass
BPF = bandpass filter
BRS = brass
BWO = backward-wave oscillator
CAL = calibrate
ccw = counterclockwise
CER = ceramic
CHAN = channel
cm = centimeter
CMO = coaxial
COEF = coefficient
COM = common
COMP = composition
COMPL = complete
CONN = connector
CP = cadmium plate
CRT = cathode-ray tube
CTL = complementary transistor logic
CW = continuous wave
cw = clockwise
D/A = digital-to-analog
dB = decibel
dBm = decibel referred to 1 mW
dc = direct current
deg = degree (temperature interval or difference)
° = degree (plane angle)
°C = degree Celsius (centigrade)
°F = degree Fahrenheit
°K = degree Kelvin
DEPC = deposited carbon
DET = detector
diam = diameter
DIA = diameter (used in parts list)
DIFF AMPL = differential amplifier
div = division
DPDT = double-pole, double-throw
DR = drive
DSB = double sideband
DTL = diode transistor logic
DVM = digital voltmeter
ECL = emitter coupled logic
EMF = electromotive force
EDP = electronic data processing
ELECT = electrolytic
ENCAP = encapsulated
EXT = external
F = farad
FET = field-effect transistor
F/F = flip-flop
FH = flat head
FOL H = fillister head
FM = frequency modulation
FP = front panel
FREQ = frequency
FXD = fixed
g = gram
GE = germanium
GHz = gigahertz
GL = glass
GND = ground(ed)
H = henry
h = hour
HET = heterodyne
HEX = hexagonal
HD = head
HDW = hardware
HF = high frequency
HG = mercury
HI = high
HP = Hewlett-Packard
HPF = high pass filter
HR = hour (used in parts list)
HV = high voltage
Hz = hertz
IC = integrated circuit
ID = inside diameter
IF = intermediate frequency
IMPG = impregnated
in = inch
INCD = incandescent
INCL = include(s)
INP = input
INS = insulation
INT = internal
kg = kilogram
kHz = kilohertz
kΩ = kilohm
kV = kilovolt
lb = pound
LC = inductance-capacitance
LED = light-emitting diode
LF = low frequency
LG = long
LH = left hand
LIM = limit
LIN = linear taper (used in parts list)
lin = linear
LK WASH = lockwasher
LO = low; local oscillator
LOG = logarithmic taper (used in parts list)
log = logarithm(ic)
LPF = low pass filter
LV = low voltage
m = metre (distance)
mA = milliampere
MAX = maximum
MΩ = megohm
MEG = meg (10^6) (used in parts list)
MET FLM = metal film
MET OX = metal oxide
MF = medium frequency; microfarad (used in parts list)
MFR = manufacturer
mg = milligram
MHz = megahertz
mH = millihenry
mho = conductance
MIN = minimum
min = minute (time)
' = minute (plane angle)
MINAT = miniature
mm = millimetre
MOD = modulator
MOM = momentary
MOS = metal-oxide semiconductor
ms = millisecond
MTG = mounting
MTR = meter (indicating device)
mV = millivolt
mVac = millivolt, ac
mVdc = millivolt, dc
mVpk = millivolt, peak
mVp-p = millivolt, peak-to-peak
mVrms = millivolt, rms
mW = milliwatt
MUX = multiplex
MY = mylar
μA = microampere
μF = microfarad
μH = microhenry
μmho = micromho
μs = microsecond
μV = microvolt
μVac = microvolt, ac
μVdc = microvolt, dc
μVpk = microvolt, peak
μVp-p = microvolt, peak-to-peak
μVrms = microvolt, rms
μW = microwatt
nA = nanoampere
NC = no connection
N/C = normally closed
NE = neon
NEG = negative
nF = nanofarad
NI PL = nickel plate
N/O = normally open
NOM = nominal
NORM = normal
NPN = negative-positive-negative
NPO = negative-positive zero (zero temperature coefficient)
NRFR = not recommended for field replacement
ns = nanosecond
NSR = not separately replaceable
nW = nanowatt
OBD = order by description
OD = outside diameter
OH = oval head
OP AMPL = operational amplifier
OPT = option
OSC = oscillator
OX = oxide
oz = ounce
Ω = ohm
P = peak (used in parts list)
PAM = pulse-amplitude modulation
PC = printed circuit
PCM = pulse-code modulation; pulse-count modulation
PDM = pulse-duration modulation
pF = picofarad
PH BRZ = phosphor bronze
PHL = phillips
PIN = positive-intrinsic-negative
PIV = peak inverse voltage
pk = peak
PL = phase lock
PLO = phase lock oscillator
PM = phase modulation
PNP = positive-negative-positive
P/O = part of
POLY = polystyrene
PORC = porcelain
POS = positive; position(s) (used in parts list)
POSN = position
POT = potentiometer
p-p = peak-to-peak
PP = peak-to-peak (used in parts list)
PPM = pulse-position modulation
PREAMPL = preamplifier
PRF = pulse-repetition frequency
PRR = pulse repetition rate
ps = picosecond
PT = point
PTM = pulse-time modulation
PWM = pulse-width modulation
PWV = peak working voltage
RC = resistance capacitance
RECT = rectifier
REF = reference
REG = regulated
REPL = replaceable
RF = radio frequency
RFI = radio frequency interference
RH = round head; right hand
RLC = resistance-inductance-capacitance
RMO = rack mount only
rms = root-mean-square
RND = round
ROM = read-only memory
R&P = rack and panel
RWV = reverse working voltage
S = scattering parameter
s = second (time)
" = second (plane angle)
S-B = slow-blow fuse (used in parts list)
SCR = silicon controlled rectifier; screw
SE = selenium
SECT = sections
SEMICON = semiconductor
SHF = superhigh frequency
SI = silicon
SIL = silver
SL = slide
SNR = signal-to-noise ratio
SPDT = single-pole, double-throw
SPG = spring
SR = split ring
SPST = single-pole, single-throw
SSB = single sideband
SST = stainless steel
STL = steel
SQ = square
SWR = standing-wave ratio
SYNC = synchronize
T = timed (slow-blow fuse)
TA = tantalum
TC = temperature compensating
TD = time delay
TERM = terminal
TFT = thin-film transistor
TGL = toggle
THD = thread
THRU = through
TI = titanium
TOL = tolerance
TRIM = trimmer
TSTR = transistor
TTL = transistor-transistor logic
TV = television
TVI = television interference
TWT = traveling wave tube
U = micro (10^{-6}) used in parts list)
UF = microfarad (used in parts list)
UHF = ultrahigh frequency
UNREG = unregulated
V = volt
VA = voltampere
Vac = volts ac
VAR = variable
VCO = voltage-controlled oscillator
Vdc = volts dc
VDCW = volts, dc, working (used in parts list)
V(F) = volts, filtered
VFO = variable-frequency oscillator
VHF = very-high frequency
Vpk = volts peak
Vp-p = volts peak-to-peak
Vrms = volts rms
VSWR = voltage standing wave ratio
VTO = voltage-tuned oscillator
VTVM = vacuum-tube voltmeter
V(X) = volts, switched
W = watt
W/ = with
WIV = working inverse voltage
WW = wirewound
W/O = without
YIG = yttrium-iron-garnet
Zo = characteristic impedance

NOTE

All abbreviations in the parts list will be in upper case.

MULTIPLIERS

Abbreviation	Prefix	Multiple
T	tera	10^{12}
G	giga	10^{9}
M	mega	10^{6}
k	kilo	10^{3}
da	deka	10
d	deci	10^{-1}
c	centi	10^{-2}
m	milli	10^{-3}
μ	micro	10^{-6}
n	nano	10^{-9}
p	pico	10^{-12}
f	femto	10^{-15}
a	atto	10^{-18}

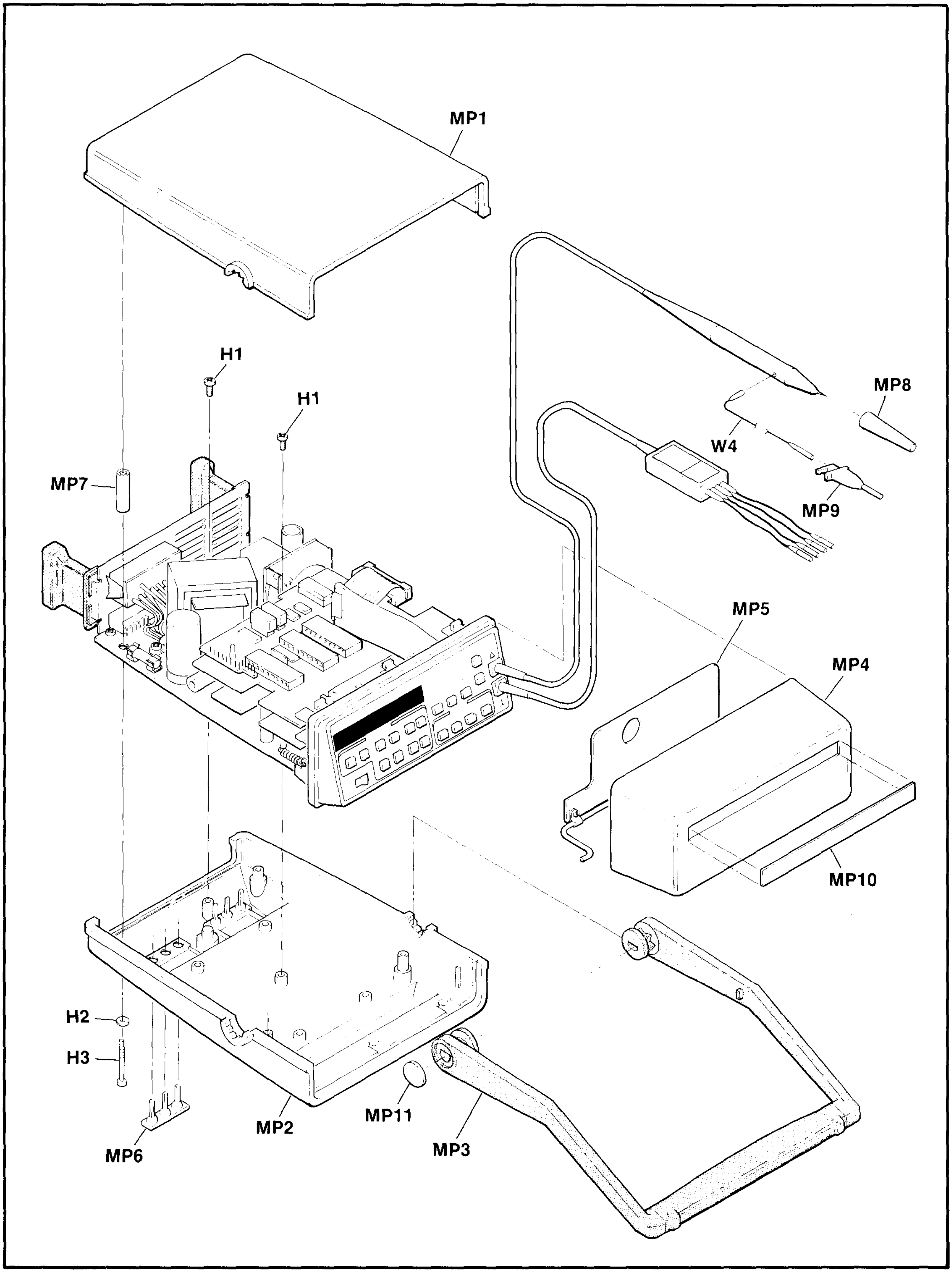

MP1
H1
H1
MP8
W4
MP7
MP9
MP5
MP4
MP10
H2
H3
MP2
MP11
MP3
MP6

Figure 6-1. Cabinet Parts and Hardware (External)

REFERENCE DESIGNATOR	HP PART NUMBER	DESCRIPTION	QUANTITY
MP1	4040-1542	SHELL, TOP	1
MP2	4040-1541	SHELL, BOTTOM	1
MP3	05005-40005	HANDLE	1
MP4	05005-40003	SAFETY COVER	1
MP5	05005-60119	SAFETY COVER, INSIDE DOOR	1
MP6	5040-7223	FOOT, BOTTOM SHELL	2
MP7	5040-8044	SPACER, BLACK PLASTIC	4
MP8	00547-40005	PROBE TIP COVER	1
MP9	10230-62101	GRABBER CONNECTOR	5
MP10	7120-8782	LABEL, SAFETY COVER	1
MP11	7120-5370	LABEL, HANDLE	1
H1	2360-0115	SCREW MACH 6-32 .312 IN LG PAN-HD-POZI	2
H2	2360-0137	SCREW MACH 6-32 1.75 IN LG PAN-HD-POZI	4
H3	2190-0018	LOCKWASHER HLCL NO. 6, .141 IN-ID	4
W4	05005-60116	PROBE GROUND CABLE	1

Part of Figure 6-1. Cabinet Parts and Hardware (External)

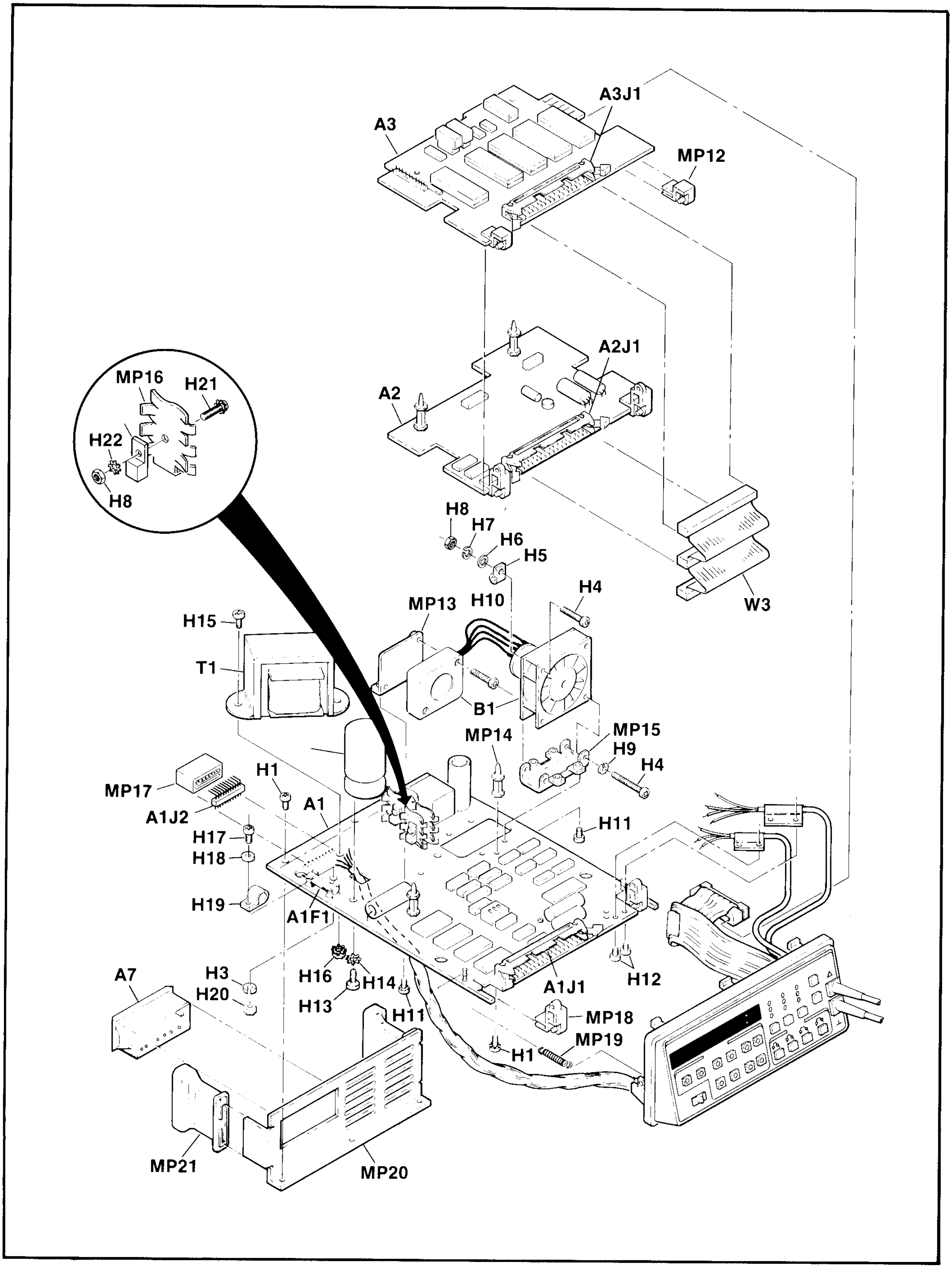

A3J1
A3
MP12
A2J1
A2
MP16
H21
H22
H8
H8
H7
H6
H5
H4
MP13
H10
W3
H15
T1
B1
MP14
MP15
H9
H4
MP17
H1
A1
A1J2
H11
H17
H18
H19
A1F1
A7
H3
H20
H16
H14
H13
H11
A1J1
H12
MP18
MP19
H1
MP21
MP20

Figure 6-2. Cabinet Parts and Hardware (Internal)

REFERENCE DESIGNATOR	HP PART NUMBER	DESCRIPTION	QUANTITY
MP12	5040-7787	HALF HINGE, PLASTIC	2
MP13	05005-00003	BRACKET, FAN MOTOR CONTROLLER	1
MP14	0380-0630	SPACER, SNAP-IN	4
MP15	05005-00002	BRACKET, FAN	1
MP16	1205-0349	HEAT SYNC	4
MP17	05005-40004	CONNECTOR, BODY	1
MP18	5040-7721	FULL HINGE, PLASTIC	4
MP19	1460-1857	SPRING	2
MP20	05005-00001	REAR PANEL	1
MP21	05005-40006	FOOT, REAR PANEL	2
H1	2360-0115	SCREW MACH 6-32 .312 IN LG PAN-HD-POZI	9
H3	2190-0018	LOCKWASHER HLCL NO. 6, .141 IN ID	1
H4	2200-0121	SCREW MACH 4-40 1.125 IN LG PAN-HD-POZI	3
H5	1400-0082	CABLE CLAMP, WHITE NYLON	1
H6	3050-0393	WASHER FLAT MTCL NO. 5, .13 IN-ID	1
H7	2190-0046	LOCKWASHER HLCL NO. 6, .141 IN-ID	1
H8	2260-0001	NUT HEX DBL-CHAM 4-40 THD .094 IN THK	5
H9	2190-0003	LOCKWASHER HLCL NO. 4, .115 IN-ID	2
H10	2200-0115	SCREW MACH 4-40 .75 IN LG PAN-HD-POZI	2
H11	2200-0103	SCREW MACH 4-40 .25 IN LG PAN-HD-POZI	6
H12	0624-0276	SCREW TAPPING 2-32 .188 IN LG PAN-HD-POZI	6
H13	2360-0128	SCREW MACH 6-32 .875 IN LG 82 DEG	2
H14	2190-0011	LOCKWASHER INTL T NO. 10, .195 IN ID	2
H15	2510-0045	SCREW MACH 8-32 .375 IN LG PAN-HD-POZI	2
H16	2500-0003	NUT HEX DBL-CHAM 6-32 THD .047 IN THK	2
H17	2360-0197	SCREW MACH 6-32 .375 IN LG PAN-HD-POZI	1
H18	3050-0001	WASHER FLAT MTLC NO. 8, .172 IN ID	1
H19	1400-0031	CABLE CLAMP, BLACK NYLON	1
H20	2500-0001	NUT HEX DBL-CHAM 6-32 THD .094 IN THK	1
H21	2200-0128	SCREW MACH 4-40 1.75 IN LG 100 DEG	4
H22	2190-0004	LOCKWASHER INTL T NO. 4, .115 IN ID	4
A1	05005-60001	MAIN ASSEMBLY	1
A2	05005-60002	DVM ASSEMBLY	1
A3	05005-60003	MICROPROCESSOR ASSEMBLY	1
A7	0960-0444	POWER LINE MODULE	1
A1B1	0950-1589	FAN AND FAN MOTOR CONTROLLER	1
A1F1	2110-0003	FUSE, 3A 250V NTD	1
A1J1	1251-6067	HEADER, 60 PIN	3
A2J1	1251-6067	HEADER, 60 PIN	1
A3J1	1251-6067	HEADER, 60 PIN	1
A1J2	1260-0814	HEADER 11 PIN	1
A1T1	9100-0465	POWER TRANSFORMER	1
C45	0180-2414	CAPACITOR, 2900 UF	1
W3	05005-60104	RIBBON CABLE, 60 LINE	1

Part of Figure 6-2. Cabinet Parts and Hardware (Internal)

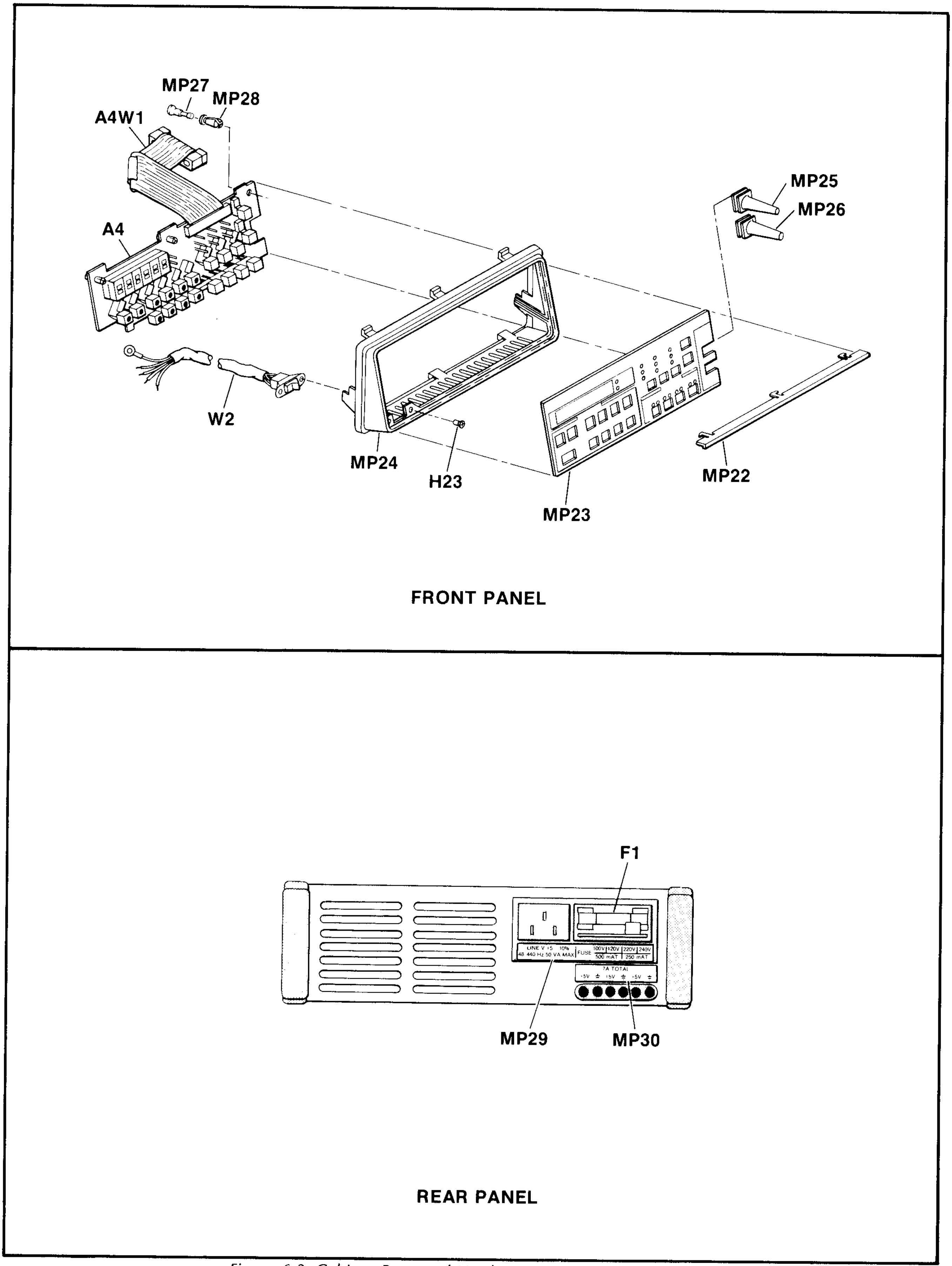

MP27
MP28
A4W1
A4
MP25
MP26
W2
MP24
H23
MP23
MP22
FRONT PANEL
F1
MP29
MP30
REAR PANEL

Figure 6-3. Cabinet Parts and Hardware (Front and Rear Panel)

REFERENCE DESIGNATOR	HP PART NUMBER	DESCRIPTION	QUANTITY
MP22	05005-40007	TRIM STRIP, FRONT PANEL	1
MP23	7101-0518	FRONT PANEL	1
MP24	05005-40002	FRONT PANEL BEZEL	1
MP25	05005-40009	BOOT, PROBE CBL	1
MP26	05005-40008	BOOT, POD CBL	1
MP27	1390-0357	LATCH PLUNGER, BLACK NYLON	3
MP28	1390-0358	LATCH GROMMET, BLACK NYLON	3
H23	2200-0140	SCREW MACH 4-40 .25 IN LG 100 DEG	2
A4	05005-60004	DISPLAY ASSEMBLY	1
A4W1	05005-60106	DISPLAY CABLE ASSEMBLY	1
W2	05005-60101	POWER CABLE ASSY	1

REFERENCE DESIGNATOR	HP PART NUMBER	DESCRIPTION	QUANTITY
MP29	7120-8788	LABEL, LINE POWER MODULE	1
MP30	7120-8787	LABEL, +5 VOLT POWER OUTPUT	1
A7F1	2110-0202	FUSE, .5A 250V TD (115V OPERATION)	1
	or		
	2110-0201	FUSE, .25A 250V TD (220V OPERATION)	1

Part of Figure 6-3. Cabinet Parts and Hardware (Front and Rear Panel)

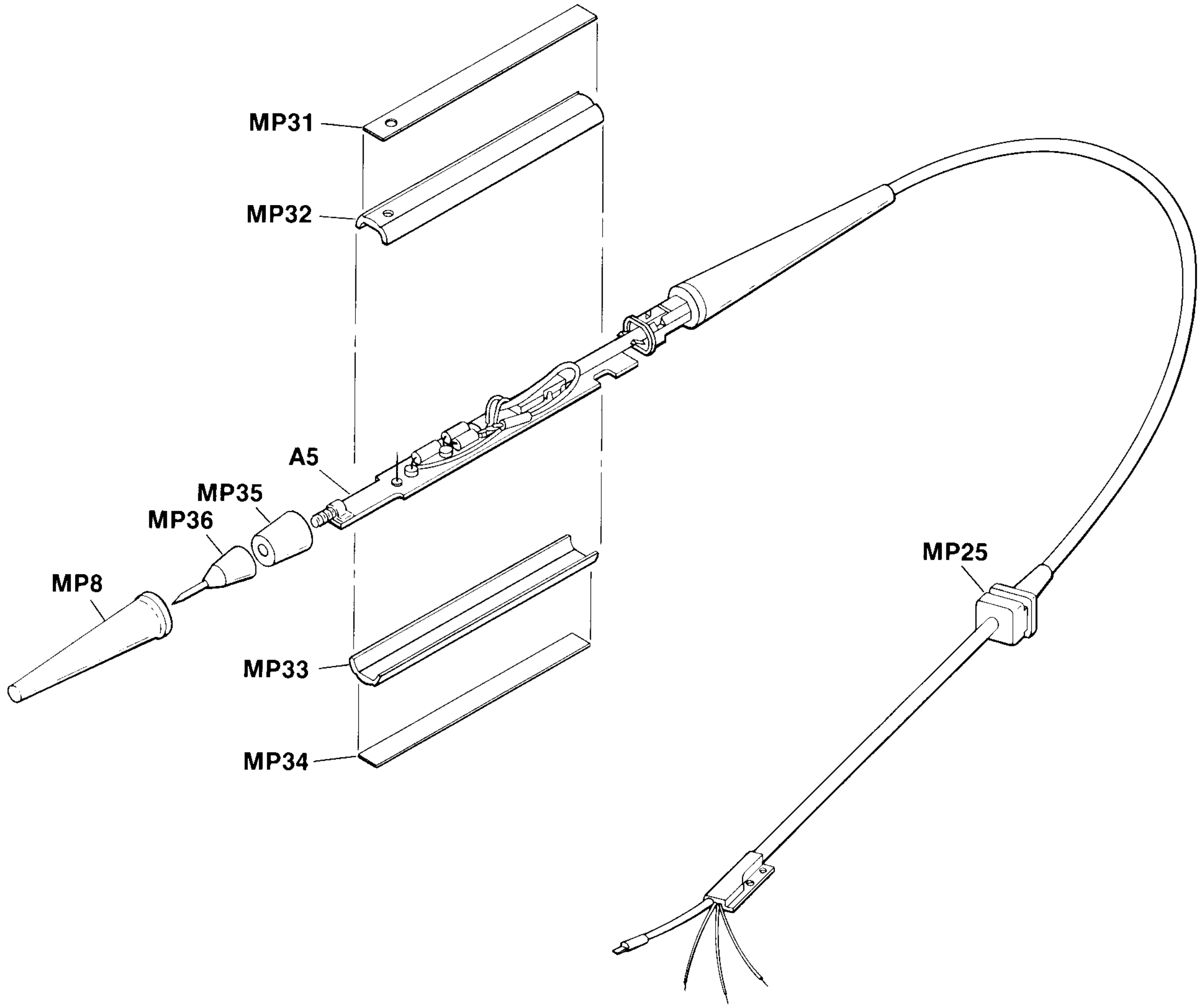

MP31
MP32
A5
MP35
MP36
MP8
MP33
MP34
MP25

Figure 6-4. Cabinet Parts and Hardware (Data Probe)

REFERENCE DESIGNATOR	HP PART NUMBER	DESCRIPTION	QUANTITY
	05005-60103	DATA PROBE AND CABLE ASSY	1
MP8	00547-40005	PROBE TIP COVER	1
MP25	05005-40009	BOOT, PROBE CABLE	1
MP31	7120-8783	LABEL, PROBE TOP W/GROUND HOLE	1
MP32	05005-20203	PROBE BODY, TOP	1
MP33	05005-20202	PROBE BODY, BOTTOM	1
MP34	7120-8786	LABEL, PROBE BOTTOM	1
MP35	00546-40002	PROBE LAMP WINDOW, RED PLASTIC	1
MP36	5060-0418	PROBE PIN TIP ASSY	1
A5	05005-60005	PROBE ASSEMBLY	1

NOTE

When repairing the Data Probe, most of the individual cabinet parts can be ordered and replaced. However, when any part of the cable assembly is damaged, the whole Data Probe and Cable assembly must be replaced. Order HP Part Number 05005-60103, which includes all the parts shown in *figure 6-4.*

Part of Figure 6-4. Cabinet Parts and Hardware (Data Probe)

CAUTION

The Timing Pod metal shield must be installed properly. The shield has an insulated plane, which must be positioned against the bottom of the pc board. When installing the shield, fold as illustrated and secure with screws to the crimped cable strain relief.

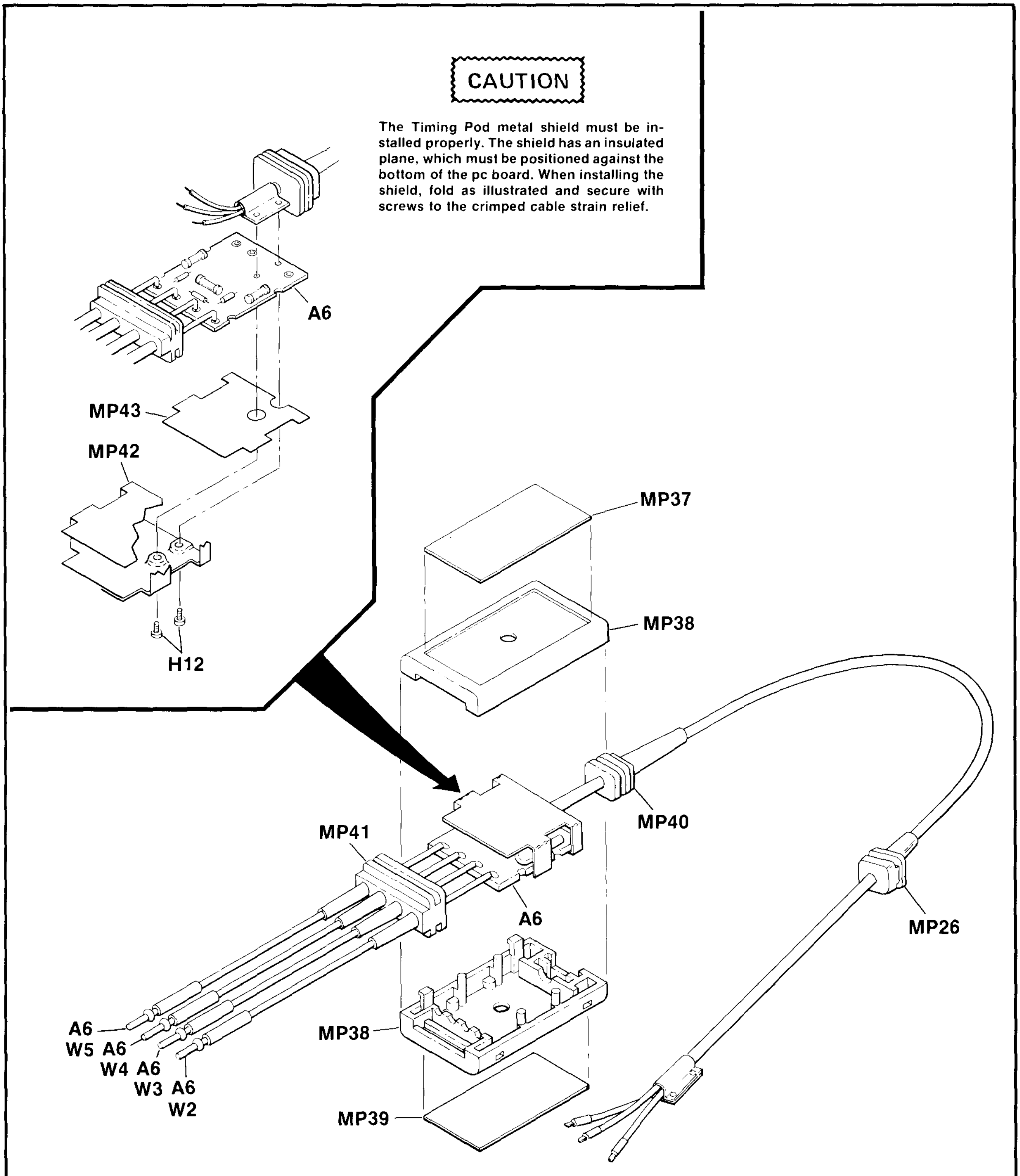

A6
MP43
MP42
H12
MP37
MP38
MP40
MP41
A6
MP26
A6
W5 A6
W4 A6
W3 A6
W2
MP38
MP39

Figure 6-5. Cabinet Parts and Hardware (Timing Pod)

REFERENCE DESIGNATOR	HP PART NUMBER	DESCRIPTION	QUANTITY
	05005-60102	TIMING POD AND CABLE ASSY	1
MP26	05005-40008	BOOT, CABLE TO FRONT PANEL	1
MP37	7120-8785	LABEL, TOP (LEFT JUSTIFIED)	1
MP38	05005-40001	POD, COVER HALF	2
MP39	7120-8784	LABEL, BOTTOM (RIGHT JUSTIFIED)	1
MP40	05005-40010	BOOT, CABLE TO POD	1
MP41	05005-40011	BOOT, TIMING LEADS TO POD	1
MP42	05005-00005	SHIELD, METAL	1
MP43	05005-00006	INSULATOR, FOR METAL SHIELD	1
H12	0624-0276	SCREW TAPPING 2-32 .188 IN LG PAN-HD-POZI	2
A6	05005-60006	TIMING POD ASSEMBLY	1
A6W2	05005-60112	POD LEAD, START	1
A6W3	05005-60113	POD LEAD, STOP	1
A6W4	05005-60114	POD LEAD, CLOCK	1
A6W5	05005-60115	POD LEAD, GROUND	1

NOTE

When repairing the Timing Pod, most of the individual cabinet parts can be ordered and replaced. However, when any part of the cable assembly is damaged, the whole Timing Pod and Cable assembly must be replaced. Order HP Part Number 05005-60102, which includes all the parts shown in *Figure 6-5.*

Part of Figure 6-5. Cabinet Parts and Hardware (Timing Pod)

Table 6-2. Replaceable Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	05005-60001	8	1	MAIN ASSEMBLY - (SERIES 2138)	28480	05005-60001
A1C1	0180-0374	3	1	CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A1C2	0160-4557	0	8	CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A1C3	0160-0576	5	8	CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C4	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C5	0160-4554	7	4	CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A1C6	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C7	0121-0061	1	1	CAPACITOR-V TRMR-CER 5.5-18PF 350V	52763	304322 5.5/18PF NPO
A1C8	0121-0114	5	3	CAPACITOR-V TRMR-CER 7-25PF 350V PC-MTG	52763	304322 7/25PF N300
A1C9	0121-0114	5		CAPACITOR-V TRMR-CER 7-25PF 350V PC-MTG	52763	304322 7/25PF N300
A1C10	0121-0114	5		CAPACITOR-V TRMR-CER 7-25PF 350V PC-MTG	52763	304322 7/25PF N300
A1C11	0160-3879	7	6	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C12	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C13	0160-3876	4	4	CAPACITOR-FXD 47PF +-20% 200VDC CER	28480	0160-3876
A1C14	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C15	0160-3876	4		CAPACITOR-FXD 47PF +-20% 200VDC CER	28480	0160-3876
A1C16	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A1C17	0160-3876	4		CAPACITOR-FXD 47PF +-20% 200VDC CER	28480	0160-3876
A1C18	0180-0418	6	1	CAPACITOR-FXD 1UF+-20% 35VDC TA	28480	0180-0418
A1C19	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C20	0160-3876	4		CAPACITOR-FXD 47PF +-20% 200VDC CER	28480	0160-3876
A1C21	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A1C22	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C23	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C24	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C25	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C26	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C27	0180-2662	6	1	CAPACITOR-FXD 10UF+-10% 10VDC TA	25088	D4R7GS1A10K
A1C28	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A1C29	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C30	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A1C31	0180-0116	1	1	CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A1C32	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
				NOT ASSIGNED		
A1C34	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A1C35	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A1C36	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A1C37	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A1C38	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A1C39	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A1C40	0180-1701	2	1	CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A1C41	0180-0197	8	1	CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A1C42	0180-2988	9	1	CAPACITOR-FXD 820UF+75-10% 40VDC AL	56289	39DX827G040GJ6
A1C43	0180-2811	7	1	CAPACITOR-FXD 10UF+-20% 35VDC TA	28480	0180-2811
A1C44	0180-2815	1	1	CAPACITOR-FXD 100UF+-20% 10VDC TA	28480	0180-2815
A1C45	0180-2414	6	1	CAPACITOR-FXD 2900UF+75-10% 40VDC AL	56289	36D292G040AA2A
A1C46	0180-2827	5	1	CAPACITOR-FXD 47UF+100-10% 40VDC AL	28480	0180-2827
A1C47	0180-2892	4	1	CAPACITOR-FXD 2200UF+75-10% 16VDC AL	28480	0180-2892
A1C48	0180-2827	5		CAPACITOR-FXD 47UF+100-10% 40VDC AL	28480	0180-2827
A1C49	0160-0572	1	1	CAPACITOR-FXD 2200PF +-20% 100VDC CER	28480	0160-0572
A1C50	0160-0573	2	1	CAPACITOR-FXD 4700PF +-20% 100VDC CER	28480	0160-0573
A1C51	0140-0207	7	1	CAPACITOR-FXD 330PF +-5% 500VDC MICA	72136	DM15F331J0500WV1CR
A1CR1	1901-0033	2	2	DIODE-GEN PRP 180V 200MA DO-7	28480	1901-0033
A1CR2	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-7	28480	1901-0033
A1CR3	1901-0731	7	2	DIODE-PWR RECT 400V 1A	28480	1901-0731
A1CR4	1901-0731	7		DIODE-PWR RECT 400V 1A	28480	1901-0731
A1CR5	1906-0069	4	2	DIODE-FW BRDG 400V 1A	28480	1906-0069
A1CR6	1906-0069	4		DIODE-FW BRDG 400V 1A	28480	1906-0069
A1CR7	1901-1086	7	1	DIODE-PWR RECT 50V 5A 200NS	04713	MR820
A1CR8	1902-0522	6	1	DIODE-ZNR 1N5340B 6V 5% PD=5W IR=1UA	04713	1N5340B
A1F1	2110-0003	0	1	FUSE 3A 250V NTD 1.25X.25 UL	75915	312003
A1J1	1251-6067	5	3	CONNECTOR 60-PIN M POST TYPE	28480	1251-6067
A1J2	1260-0814	7	1	HEADER-TERM	28480	1260-0814
A1K1	0490-1220	7	1	RELAY-REED 1A 500MA 250VDC 5VDC-COIL	28480	0490-1220
A1K2	0490-1219	4	1	RELAY-REED 1C 500MA 250VDC 5VDC-COIL	28480	0490-1219
A1L1	9100-2276	9	1	INDUCTOR RF-CH-MLD 100UH 10% .105DX.26LG	28480	9100-2276
A1L2	9100-3017	8	1	300 MH AT 5 AMP DC	28480	9100-3017
A1Q1	1854-0215	1	1	TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1Q2	1853-0363	8	1	TRANSISTOR PNP SI PD=50W FT=20MHZ	03508	X45H281

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts List (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1R1	0698-6360	6	4	RESISTOR 10K .1% .125W F TC=0+-25	28480	0698-6360
A1R2	0698-7207	2	3	RESISTOR 61.9 1% .05W F TC=0+-100	24546	C3-1/8-T00-61R9-G
A1R3	0698-7227	6	3	RESISTOR 422 1% .05W F TC=0+-100	24546	C3-1/8-T0-422R-G
A1R4	0698-6630	3	8	RESISTOR 20K .1% .125W F TC=0+-25	28480	0698-6630
A1R5	0698-6630	3		RESISTOR 20K .1% .125W F TC=0+-25	28480	0698-6630
A1R6	0698-0084	9	1	RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A1R7	0698-3439	4	1	RESISTOR 178 1% .125W F TC=0+-100	24546	C4-1/8-T0-178R-F
A1R8	0698-6360	6		RESISTOR 10K .1% .125W F TC=0+-25	28480	0698-6360
A1R9	0698-7205	0	1	RESISTOR 51.1 1% .05W F TC=0+-100	24546	C3-1/8-T00-51R1-G
A1R10	0698-6360	6	1	RESISTOR 10K .1% .125W F TC=0+-25	28480	0698-6360
A1R11	0698-7227	6		RESISTOR 422 1% .05W F TC=0+-100	24546	C3-1/8-T0-422R-G
A1R12	0698-7207	2		RESISTOR 61.9 1% .05W F TC=0+-100	24546	C3-1/8-T00-61R9-G
A1R13	0698-7227	6		RESISTOR 422 1% .05W F TC=0+-100	24546	C3-1/8-T0-422R-G
A1R14	0698-7207	2		RESISTOR 61.9 1% .05W F TC=0+-100	24546	C3-1/8-T00-61R9-G
A1R15	0698-6360	6		RESISTOR 10K .1% .125W F TC=0+-25	28480	0698-6360
A1R16	0698-6630	3		RESISTOR 20K .1% .125W F TC=0+-25	28480	0698-6630
A1R17	0698-6619	8	4	RESISTOR 15K .1% .125W F TC=0+-25	28480	0698-6619
A1R18	0698-6348	0	4	RESISTOR 3K .1% .125W F TC=0+-25	28480	0698-6348
A1R19	0698-6619	8		RESISTOR 15K .1% .125W F TC=0+-25	28480	0698-6619
A1R20	0698-6413	0	4	RESISTOR 6.5K .1% .125W F TC=0+-25	28480	0698-6413
A1R21	0698-6413	0		RESISTOR 6.5K .1% .125W F TC=0+-25	28480	0698-6413
A1R22	0698-6348	0		RESISTOR 3K .1% .125W F TC=0+-25	28480	0698-6348
A1R23	0698-6413	0		RESISTOR 6.5K .1% .125W F TC=0+-25	28480	0698-6413
A1R24	0698-6413	0		RESISTOR 6.5K .1% .125W F TC=0+-25	28480	0698-6413
A1R25	1810-0374	1	1	NETWORK-RES 8-SIP1.0K OHM X 4	01121	208B102
A1R26	0698-6630	3		RESISTOR 20K .1% .125W F TC=0+-25	28480	0698-6630
A1R27	0698-6619	8		RESISTOR 15K .1% .125W F TC=0+-25	28480	0698-6619
A1R28	0698-6348	0		RESISTOR 3K .1% .125W F TC=0+-25	28480	0698-6348
A1R29	0698-6619	8		RESISTOR 15K .1% .125W F TC=0+-25	28480	0698-6619
A1R30	0698-6348	0		RESISTOR 3K .1% .125W F TC=0+-25	28480	0698-6348
A1R31	0698-6630	3		RESISTOR 20K .1% .125W F TC=0+-25	28480	0698-6630
A1R32	0698-3989	9	8	RESISTOR 3.84K .1% .125W F TC=0+-25	28480	0698-3989
A1R33	0698-3989	9		RESISTOR 3.84K .1% .125W F TC=0+-25	28480	0698-3989
A1R34	0698-3989	9		RESISTOR 3.84K .1% .125W F TC=0+-25	28480	0698-3989
A1R35	0698-6630	3		RESISTOR 20K .1% .125W F TC=0+-25	28480	0698-6630
A1R36	1810-0273	9	1	NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A1R37	0698-3989	9		RESISTOR 3.84K .1% .125W F TC=0+-25	28480	0698-3989
A1R38	0698-3989	9		RESISTOR 3.84K .1% .125W F TC=0+-25	28480	0698-3989
A1R39	0698-3989	9		RESISTOR 3.84K .1% .125W F TC=0+-25	28480	0698-3989
A1R40	0698-6630	3		RESISTOR 20K .1% .125W F TC=0+-25	28480	0698-6630
A1R41	0757-0280	3	6	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R42	0698-6630	3		RESISTOR 20K .1% .125W F TC=0+-25	28480	0698-6630
A1R43				NOT ASSIGNED		
A1R44	0698-3989	9		RESISTOR 3.84K .1% .125W F TC=0+-25	28480	0698-3989
A1R45	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R46	0698-3989	9		RESISTOR 3.84K .1% .125W F TC=0+-25	28480	0698-3989
A1R47	0698-3988	8	2	RESISTOR 42K .1% .125W F TC=0+-25	28480	0698-3988
A1R48	0698-3988	8		RESISTOR 42K .1% .125W F TC=0+-25	28480	0698-3988
A1R49	0698-3987	7	1	RESISTOR 70K .1% .125W F TC=0+-25	28480	0698-3987
A1R50	0698-3959	3	1	RESISTOR 80K .1% .25W F TC=0+-25	28480	0698-3959
A1R51	0698-6977	1	1	RESISTOR 30K .1% .125W F TC=0+-25	28480	0698-6977
A1R52	0811-3114	4	2	RESISTOR 75 3% 5W PW TC=0+-20	28480	0811-3114
A1R53	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R54	0757-0419	0	1	RESISTOR 681 1% .125W F TC=0+-100	24546	C4-1/8-T0-681R-F
A1R55	0698-3447	4	1	RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
A1R56	0698-3391	7	1	RESISTOR 21.5 1% .5W F TC=0+-100	28480	0698-3391
A1R57	0811-3114	4		RESISTOR 75 3% 5W PW TC=0+-20	28480	0811-3114
A1R58	0811-3288	3	1	RESISTOR .025 10% 2W PW TC=0+-180	28480	0811-3288
A1R59	0757-0394	0	1	RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A1R60	0757-0199	3	1	RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
A1R61	0698-5218	1	1	RESISTOR 30K .5% .125W F TC=0+-100	24546	C4-1/8-T0-3002-D
A1R62	0757-0401	0	1	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A1R63	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R64	0698-4002	9	1	RESISTOR 5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5001-F
A1R65	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R66	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1S1	3101-0488	7	1	SWITCH-SL 3-SPDT DIP-SLIDE-ASSY .1A	28480	3101-0488
A1TP1	1251-4707	6	5	CONNECTOR-SGL CONT PIN .031-IN-BSC-SZ	28480	1251-4707
A1TP2	1251-4707	6		CONNECTOR-SGL CONT PIN .031-IN-BSC-SZ	28480	1251-4707
A1TP3	1251-4707	6		CONNECTOR-SGL CONT PIN .031-IN-BSC-SZ	28480	1251-4707
A1TP4	1251-4707	6		CONNECTOR-SGL CONT PIN .031-IN-BSC-SZ	28480	1251-4707
A1TP5	1251-4707	6		CONNECTOR-SGL CONT PIN .031-IN-BSC-SZ	28480	1251-4707
A1U1	1826-0659	8	4	IC CONV 8-B-D/A 24-DIP-P PKG	34335	AM6081PC
A1U2	1820-1281	2	1	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS139N
A1U3	1820-0998	6	1	IC MUXR/DATA-SEL TTL S 4-TO-1-LINE DUAL	01295	SN74S153N
A1U4	1826-0659	8		IC CONV 8-B-D/A 24-DIP-P PKG	34335	AM6081PC
A1U5	1820-1639	4	1	IC GATE TTL S EXCL-OR/NOR QUAD 2-INP	01295	SN74S135N

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts List (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1U6	1826-0630	5	1	IC COMPARATOR HS	28480	1826-0630
A1U7	1826-0659	8		IC CONV 8-B-D/A 24-DIP-P PKG	34335	AM6081PC
A1U8	1820-1453	0	4	IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	01295	SN74S163N
A1U9	1820-1453	0		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	01295	SN74S163N
A1U10	1820-0629	0	3	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
A1U11	1820-1052	5	2	IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
A1U12	1820-1052	5		IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
A1U13	1826-0659	8		IC CONV 8-B-D/A 24-DIP-P PKG	34335	AM6081PC
A1U14	1826-0522	4	1	IC OP AMP QUAD 14-DIP-P PKG	01295	TL074CN
A1U15	1820-1453	0		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	01295	SN74S163N
A1U16	1820-1319	7	1	IC MUXR/DATA-SEL TTL S 8-TO-1-LINE 8-INP	01295	SN74S151N
A1U17	1820-0694	9	1	IC GATE TTL S EXCL-OR QUAD 2-INP	01295	SN74S86N
A1U18	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
A1U19	1820-1453	0		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	01295	SN74S163N
A1U20	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
A1U21	1820-0693	8	1	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A1U22	1820-1015	0	1	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
A1U23	1826-0038	7	1	IC OP AMP SPCL TO-99 PKG	04713	MC1436G
A1U24	1820-1610	1	1	IC-VOLTAGE REGULATOR-SWITCHING	28480	1820-1610
A1U25	1826-0565	5	1	IC-LOGIC PROBE PROCESSOR	28480	1826-0565
A1U26	1820-0681	4	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
A1VR1	1826-0221	0	1	IC V RGLTR TO-220	04713	MC7912CT
A1VR2	1826-0215	2	1	IC V RGLTR TO-220	04713	MC7905.2CT
A1VR3	1826-0147	9	1	IC 7812 V RGLTR TO-220	04713	MC7812CP
A1W2	05005-60117	7	1	CABLE ASSEMBLY-RED JUMPER	28480	05005-60117
A1W3	05005-60118	8	1	CABLE ASSEMBLY-GREEN JUMPER	28480	05005-60118
A1W4	05005-60105	3	1	CABLE ASSEMBLY-BLACK JUMPER	28480	05005-60105
				A1 MISCELLANEOUS PARTS		
	0340-0060	4	3	TERMINAL-STUD SPCL-FDTHRU PRESS-MTG	98291	011-6809 000 209
	0361-0071	1	2	TERMINAL-STUD DBL-TUR SWGFRM-MTG	28480	0361-0071
MP14	0380-0630	8	2	SPACER-SNAP-IN .75 IN LG; .31 IN A/F	28480	0380-0630
MP16	1205-0349	7	4	HEAT SINK SGL PLSTC-PWR-CS	13103	6025B-TT
	2110-0269	0	2	FUSEHOLDER-CLIP TYPE.250-FUSE	28480	2110-0269
MP18	5040-7721	7	2	HINGE-FULL	28480	5040-7721
A2	05005-60002	9	1	DVM ASSEMBLY - (SERIES 1928)	28480	05005-60002
A2C1	0180-0116	1	5	CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A2C2	0160-4554	7	1	CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A2C3	0180-0229	7	4	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A2C4	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A2C5	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A2C6	0160-5027	1	1	CAPACITOR-FXD .0012UF 400VDC	28480	0160-5027
A2C7	0160-3468	0	1	CAPACITOR-FXD .12UF +-10% 80VDC POLYE	28480	0160-3468
A2C8	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A2C9	0160-4557	0	2	CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A2C10	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A2C11	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A2C12	0180-2617	1	3	CAPACITOR-FXD 6.8UF+-10% 35VDC TA	25088	D6R8GS1B35K
A2C13	0180-2617	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	25088	D6R8GS1B35K
A2C14	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A2C15	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A2C16	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A2C17	0180-2617	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	25088	D6R8GS1B35K
A2CR1	1901-0731	7	2	DIODE-PWR RECT 400V 1A	28480	1901-0731
A2CR2	1901-0731	7		DIODE-PWR RECT 400V 1A	28480	1901-0731
A2CR3	1901-0376	6	4	DIODE-GEN PRP 35V 50MA DO-35	28480	1901-0376
A2CR4	1901-0376	6		DIODE-GEN PRP 35V 50MA DO-35	28480	1901-0376
A2CR5	1901-0376	6		DIODE-GEN PRP 35V 50MA DO-35	28480	1901-0376
A2CR6	1901-0376	6		DIODE-GEN PRP 35V 50MA DO-35	28480	1901-0376
A2CR7	1901-0033	2	1	DIODE-GEN PRP 180V 200MA DO-7	28480	1901-0033
A2J1	1251-6067	5	1	HEADER-60 PIN	28480	1251-6067
A2K1	0490-1219	4	1	RELAY-REED 1C 500MA 250VDC 5VDC-COIL	28480	0490-1219
A2K2	0490-1220	7	1	RELAY-REED 1A 500MA 250VDC 5VDC-COIL	28480	0490-1220
A2L1	9100-1788	6	2	CHOKE-WIDE BAND ZMAX=680 OHM@ 180 MHZ	02114	VK200 20/48
A2L2	9100-1788	6		CHOKE-WIDE BAND ZMAX=680 OHM@ 180 MHZ	02114	VK200 20/48
A2Q1	05005-80001	0	4	TRANSISTOR-FET (SEALED)	28480	05005-80001
A2Q2	05005-80001	0		TRANSISTOR-FET (SEALED)	28480	05005-80001
A2Q3	05005-80001	0		TRANSISTOR-FET (SEALED)	28480	05005-80001
A2Q4	05005-80001	0		TRANSISTOR-FET (SEALED)	28480	05005-80001
A2Q5	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts List (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2Q6	1853-0036	2	1	TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A2R1	0698-6369	5	1	RESISTOR 1M .1% .25W F TC=0+-25	28480	0698-6369
A2R2	2100-3161	6	1	RESISTOR-TRMR 20K 10% C SIDE-ADJ 17-TRN	02111	43P203
A2R3	0757-0200	7	1	RESISTOR 5.62K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5621-F
A2R4	0698-3986	6	1	RESISTOR 89K .1% .125W F TC=0+-25	28480	0698-3986
A2R5	0699-0073	8	1	RESISTOR 10M 1% .125W F TC=0+-150	28480	0699-0073
A2R6	0698-3960	6	1	RESISTOR 1.1M 1% .125W F TC=0+-100	28480	0698-3960
A2R7	0757-0465	6	1	RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A2R8	0698-6612	1	2	RESISTOR 2K .1% .125W F TC=0+-50	28480	0698-6612
A2R9	0698-6612	1		RESISTOR 2K .1% .125W F TC=0+-50	28480	0698-6612
A2R10	0698-6625	6	1	RESISTOR 6K .1% .125W F TC=0+-25	28480	0698-6625
A2R11	0757-0442	9	7	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A2R12	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A2R13	0699-0283	2	1	RESISTOR 81.92K .1% .125W F TC=0+-25	28480	0699-0283
A2R14	0757-0462	3	1	RESISTOR 75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7502-F
A2R15	0698-3158	4	1	RESISTOR 23.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2372-F
A2R16	0698-0085	0	1	RESISTOR 2.61K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2611-F
A2R17	0698-6358	2	1	RESISTOR 100K .1% .125W F TC=0+-25	28480	0698-6358
A2R18	0757-0280	3	4	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R19	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R20	0757-0449	6	1	RESISTOR 20K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2002-F
A2R21	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R22	0757-0458	7	1	RESISTOR 51.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5112-F
A2R23	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A2R24	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A2R25	0698-0084	9	4	RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A2R26	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A2R27	0757-0439	4	1	RESISTOR 6.81K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6811-F
A2R28	0757-0440	7	1	RESISTOR 7.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7501-F
A2R29	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A2R30	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A2R31	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A2R32	0757-0447	4	1	RESISTOR 16.2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1622-F
A2R33	0698-3444	1	1	RESISTOR 316 1% .125W F TC=0+-100	24546	C4-1/8-T0-316R-F
A2R34	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R35	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A2R36	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A2U1	1826-0650	9	1	IC-V RGLTR V-REF ADJ 2.5/10V TO-99	28480	1826-0650
A2U2	1826-0658	7	1	IC SWITCH 16-DIP-P PKG	0192B	CD22100E
A2U3	1826-0543	9	1	IC OP AMP LOW-DRIFT TO-99 PKG	06665	OP-07CJ
A2U4	1826-0588	2	1	IC CONV 16-DIP-P PKG	17856	LD120CJ
A2U5	1820-2326	8	1	IC XLTR CMOS TTL-TO-MOS HEX	04713	MC14504BCP
A2U6	1826-0412	1	1	IC COMPARATOR PRCN DUAL 8-DIP-P PKG	27014	LM393N
A2U7	1826-0587	1	1	IC CONV 18-DIP-P PKG	17856	LD121CJ
A2U8	1820-1430	3	2	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A2U9	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
				A2 MISCELLANEOUS PARTS		
	0340-0060	4	10	TERMINAL-STUD SPCL-FDTHRU PRESS-MTG	98291	011-6809 000 209
MP14	0380-0630	8	2	SPACER-SNAP-IN .75 IN LG; .31 IN A/F	28480	0380-0630
	1251-0600	0	5	CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
MP18	5040-7721	7	2	HINGE-FULL	28480	5040-7721
TP3-7	1251-4303	8	1	CONNECTOR 15-PIN (5-PINS USED)	28480	1251-4303
A3	05005-60003	0	1	MICROPROCESSOR ASSEMBLY - (SERIES 2112)	28480	05005-60003
A3C1	0180-0374	3	2	CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A3C2	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A3C3	0160-4554	7	7	CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A3C4	0180-2816	2	2	CAPACITOR-FXD 68UF+-20% 10VDC TA	28480	0180-2816
A3C5	0180-2816	2		CAPACITOR-FXD 68UF+-20% 10VDC TA	28480	0180-2816
A3C6	0160-0127	2	1	CAPACITOR-FXD 1UF +-20% 25VDC CER	28480	0160-0127
A3C7	0160-4557	0	3	CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A3C8	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A3C9	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A3C10	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A3C11	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A3C12	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A3C13	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A3C14	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A3C15	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A3C16	0180-0230	0	1	CAPACITOR-FXD 1UF+-20% 50VDC TA	56289	150D105X0050A2

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts List (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3CR1	1901-0518	8	1	DIODE-SM SIG SCHOTTKY	28480	1901-0518
A3CR2	1901-0040	1	1	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A3J1	1251-6067	5		HEADER-60 PIN	28480	1251-6067
A3Q1	1854-0215	1	1	TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A3R1	0698-8812	7	1	RESISTOR 1 1% .125W F TC=0+-100	28480	0698-8812
A3R2	0698-7244	7	3	RESISTOR 2.15K 1% .05W F TC=0+-100	24546	C3-1/8-T0-2151-G
A3R3	0698-7244	7		RESISTOR 2.15K 1% .05W F TC=0+-100	24546	C3-1/8-T0-2151-G
A3R4	1810-0369	4	1	NETWORK-RES 6-SIP100.0K OHM X 5	11236	750-61-R100K
A3R5	0698-7252	7	2	RESISTOR 4.64K 1% .05W F TC=0+-100	24546	C3-1/8-T0-4641-G
A3R6	0698-7257	2	2	RESISTOR 7.5K 1% .05W F TC=0+-100	24546	C3-1/8-T0-7501-G
A3R7	0698-7257	2		RESISTOR 7.5K 1% .05W F TC=0+-100	24546	C3-1/8-T0-7501-G
A3R8	0698-7252	7		RESISTOR 4.64K 1% .05W F TC=0+-100	24546	C3-1/8-T0-4641-G
A3R9	0698-7231	2	7	RESISTOR 619 1% .05W F TC=0+-100	24546	C3-1/8-T0-619R-G
A3R10	0698-7231	2		RESISTOR 619 1% .05W F TC=0+-100	24546	C3-1/8-T0-619R-G
A3R11	0698-7231	2		RESISTOR 619 1% .05W F TC=0+-100	24546	C3-1/8-T0-619R-G
A3R12	0698-7231	2		RESISTOR 619 1% .05W F TC=0+-100	24546	C3-1/8-T0-619R-G
A3R13	0698-7231	2		RESISTOR 619 1% .05W F TC=0+-100	24546	C3-1/8-T0-619R-G
A3R14	0698-7231	2		RESISTOR 619 1% .05W F TC=0+-100	24546	C3-1/8-T0-619R-G
A3R15	0698-7231	2		RESISTOR 619 1% .05W F TC=0+-100	24546	C3-1/8-T0-619R-G
A3R16	0698-7246	9	1	RESISTOR 2.61K 1% .05W F TC=0+-100	24546	C3-1/8-T0-2611-G
A3R17	0698-7244	7		RESISTOR 2.15K 1% .05W F TC=0+-100	24546	C3-1/8-T0-2151-G
A3R18	0698-7233	4	1	RESISTOR 750 1% .05W F TC=0+-100	24546	C3-1/8-T0-750R-G
A3R19	0698-7220	9	1	RESISTOR 215 1% .05W F TC=0+-100	24546	C3-1/8-T0-215R-G
A3R20	0698-7236	7	2	RESISTOR 1K 1% .05W F TC=0+-100	24546	C3-1/8-T0-1001-G
A3R21	1810-0368	3	1	NETWORK-RES 6-SIP10.0K OHM X 5	01121	206A103
A3R22				NOT ASSIGNED		
A3R23	0698-7260	7	3	RESISTOR 10K 1% .05W F TC=0+-100	24546	C3-1/8-T0-1002-G
A3R24	0698-7260	7		RESISTOR 10K 1% .05W F TC=0+-100	24546	C3-1/8-T0-1002-G
A3R25	0698-7270	9	1	RESISTOR 26.1K 1% .05W F TC=0+-100	24546	C3-1/8-T0-2612-G
A3R26	0698-7236	7		RESISTOR 1K 1% .05W F TC=0+-100	24546	C3-1/8-T0-1001-G
A3R27	1810-0206	8	1	NETWORK-RES 8-SIP10.0K OHM X 7	01121	208A103
A3R28	0698-7260	7		RESISTOR 10K 1% .05W F TC=0+-100	24546	C3-1/8-T0-1002-G
A3R29	0698-7284	5	1	RESISTOR 100K 1% .05W F TC=0+-100	24546	C3-1/8-T0-1003-G
A3S1	3100-3364	2	2	SWITCH-ROTARY 16 PIN DIP 4PDT	28480	3100-3364
A3S2	3100-3364	2		SWITCH-ROTARY 16 PIN DIP 4PDT	28480	3100-3364
A3U1	1813-0139	2	1	IC OSC HYBRID	34344	K1100A-10.0MHZ
A3U2	1820-1052	5	1	IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
A3U3	1820-2309	7	1	IC ENCDR CMOS	27014	MM74C923N
A3U4	1818-1542	3	1	ROM	28480	1818-1542
A3U5	1820-1112	8	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A3U6	1820-2132	4	1	IC DRVR CMOS LED DRVR	32293	ICM7218A
A3U7	1820-0174	0	2	IC INV TTL HEX	01295	SN7404N
A3U8	1818-0696	6	1	IC NMOS 2048 (2K) RAM STAT 400-NS	28480	1818-0696
A3U9	1820-1208	3	1	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
A3U10	1820-0174	0		IC INV TTL HEX	01295	SN7404N
A3U11	1818-1543	4	1	ROM	28480	1818-1543
A3U12	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A3U13	1818-1544	5	1	ROM	28480	1818-1544
A3U14	1820-2075	4	1	IC MISC TTL LS	01295	SN74LS245N
A3U15	1820-1245	8	1	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS155N
A3U16	1820-2074	3	1	IC MICPROC NMOS 8-BIT	34649	P8085
A3XS1	1200-0607	0	2	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A3XS2	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A3XU4	1200-0654	7	5	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A3XU6	1200-0567	1	1	SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
A3XU8	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A3XU11	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A3XU13	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A3XU16	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
				A3 MISCELLANEOUS PARTS		
	1251-4303	8	1	CONNECTOR-15 PIN MALE POST TYPE	28480	1251-4303
MP12	5040-7787	5	2	HINGE-HALF	28480	5040-7787
A4	05005-60004	1	1	DISPLAY ASSEMBLY - (SERIES 1928)	28480	05005-60004
A4DS1	1990-0730	3	6	DISPLAY-NUM-SEG 1-CHAR .3-H RED	28480	5082-7611
A4DS2	1990-0730	3		DISPLAY-NUM-SEG 1-CHAR .3-H RED	28480	5082-7611
A4DS3	1990-0730	3		DISPLAY-NUM-SEG 1-CHAR .3-H RED	28480	5082-7611
A4DS4	1990-0730	3		DISPLAY-NUM-SEG 1-CHAR .3-H RED	28480	5082-7611
A4DS5	1990-0730	3		DISPLAY-NUM-SEG 1-CHAR .3-H RED	28480	5082-7611

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts List (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4DS6	1990-0730	3		DISPLAY-NUM-SEG 1-CHAR .3-H RED	28480	5082-7611
A4DS7	1990-0582	3	10	LED-LAMP LUM-INT=3MCD IF=20MA-MAX BVR=5V	28480	5082-4160
A4DS8	1990-0582	3		LED-LAMP LUM-INT=3MCD IF=20MA-MAX BVR=5V	28480	5082-4160
A4DS9	1990-0582	3		LED-LAMP LUM-INT=3MCD IF=20MA-MAX BVR=5V	28480	5082-4160
A4DS10	1990-0582	3		LED-LAMP LUM-INT=3MCD IF=20MA-MAX BVR=5V	28480	5082-4160
A4DS11	1990-0582	3		LED-LAMP LUM-INT=3MCD IF=20MA-MAX BVR=5V	28480	5082-4160
A4DS12	1990-0582	3		LED-LAMP LUM-INT=3MCD IF=20MA-MAX BVR=5V	28480	5082-4160
A4DS13	1990-0582	3		LED-LAMP LUM-INT=3MCD IF=20MA-MAX BVR=5V	28480	5082-4160
A4DS14	1990-0582	3		LED-LAMP LUM-INT=3MCD IF=20MA-MAX BVR=5V	28480	5082-4160
A4DS15	1990-0665	3	20	LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0665
A4DS16	1990-0665	3		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0665
A4DS17	1990-0582	3		LED-LAMP LUM-INT=3MCD IF=20MA-MAX BVR=5V	28480	5082-4160
A4DS18	1990-0582	3		LED-LAMP LUM-INT=3MCD IF=20MA-MAX BVR=5V	28480	5082-4160
A4DS19	1990-0665	3		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0665
A4DS20	1990-0665	3		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0665
A4DS21	1990-0665	3		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0665
A4DS22	1990-0665	3		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0665
A4DS23	1990-0665	3		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0665
A4DS24	1990-0665	3		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0665
A4DS25	1990-0665	3		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0665
A4DS26	1990-0665	3		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0665
A4DS27	1990-0665	3		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0665
A4DS28	1990-0665	3		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0665
A4DS29	1990-0665	3		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0665
A4DS30	1990-0665	3		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0665
A4DS31	1990-0665	3		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0665
A4DS32	1990-0665	3		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0665
A4DS33	1990-0665	3		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0665
A4DS34	1990-0665	3		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0665
A4DS35	1990-0665	3		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0665
A4DS36	1990-0665	3		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0665
A4S1	5060-9436	7	19	PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A4S2	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A4S3	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A4S4	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A4S5	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A4S6	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A4S7	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A4S8	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A4S9	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A4S10	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A4S11	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A4S12	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A4S13	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A4S14	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A4S15	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A4S16	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A4S17	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A4S18	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A4S19	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A4W1	05005-60106	4	1	CABLE ASSEMBLY-DISPLAY	28480	05005-60106
A4W1P1	0360-1636	4	1	CABLE TRANSITION 34-TERM INSUL DSPL TYPE	28480	0360-1636
A4XD1	1200-0424	9	6	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0424
A4XD2	1200-0424	9		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0424
A4XD3	1200-0424	9		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0424
A4XD4	1200-0424	9		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0424
A4XD5	1200-0424	9		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0424
A4XD6	1200-0424	9		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0424
				A4 MISCELLANEOUS PARTS		
MP27	1390-0357	8	3	FASTENER-SNAP-IN PLGR FOR TOTAL PANEL	28480	1390-0357
MP28	1390-0358	9	3	FASTENER-SNAP-IN GROM FOR TOTAL PANEL	28480	1390-0358
	4040-1617	7	18	STANDOFF SPACER (LED)	28480	4040-1617
A5A1	05005-60005	2	1	BOARD ASSEMBLY-PROBE - (SERIES 1929)	28480	05005-60005
A5A1C1	0160-2253	9	1	CAPACITOR-FXD 6.8PF +-.25PF 500VDC CER	28480	0160-2253
A5A1DS1	2140-0346	7	1	LAMP-INCAND 7210 5VDC 33MA T-1-BULB	1F556	7210
A5A1R1	0698-3985	5	1	RESISTOR 89.6K .1% .25W F TC=0+-25	28480	0698-3985
A5A1R2	0698-7496	1	1	RESISTOR 20K .1% .25W F TC=0+-25	19701	MF52C1/4-T9-2002-B

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts List (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
				A5 MISCELLANEOUS PARTS		
				NOTE When repairing the Data Probe, most of the individual cabinet parts can be ordered and replaced. However, when any part of the cable assembly is damaged, the whole Data Probe and Cable assembly must be replaced. Order HP Part Number 05005-60103, which includes all the parts shown in Figure 6-4.		
	05005-60103	1	1	CABLE ASSEMBLY PROBE	28480	05005-60103
MP8	00547-40005	5	1	COVER TIP	28480	00547-40005
MP31	7120-8783	5	1	TOP LABEL	28480	7120-8783
MP32	05005-20203	8	1	BODY-TOP HALF	28480	05005-20203
MP33	05005-20202	7	1	BODY-BOTTOM HALF	28480	05005-20202
MP34	7120-8786	8	1	BOTTOM LABEL	28480	7120-8786
MP35	00546-40002	1	1	WINDOW	28480	00546-40002
MP36	5060-0418	7	1	PIN TIP ASSEMBLY	28480	5060-0418
	0570-0662	9	1	STUD-PROBE TIP	28480	0570-0662
A6A1	05005-60006	3	1	BOARD ASSEMBLY-POD (SERIES 1928)	28480	05005-60006
A6A1C1	0160-2252	8	3	CAPACITOR-FXD 6.2PF ±.25PF 500VDC CER	28480	0160-2252
A6A1C2	0160-2252	8		CAPACITOR-FXD 6.2PF ±.25PF 500VDC CER	28480	0160-2252
A6A1C3	0160-2252	8		CAPACITOR-FXD 6.2PF ±.25PF 500VDC CER	28480	0160-2252
A6A1R1	0698-3986	6	3	RESISTOR 89K .1% .125W F TC=0±25	28480	0698-3986
A6A1R2	0698-3986	6		RESISTOR 89K .1% .125W F TC=0±25	28480	0698-3986
A6A1R3	0698-7231	2	3	RESISTOR 619 .1% .05W F TC=0±100	24546	C3-1/8-TO-619R-G
A6A1R4	0698-7231	2		RESISTOR 619 .1% .05W F TC=0±100	24546	C3-1/8-TO-619R-G
A6A1R5	0698-3986	6		RESISTOR 89K .1% .125W F TC=0±25	28480	0698-3986
A6A1R6	0698-7231	2		RESISTOR 619 .1% .125W F TC=0±25	24546	C3-1/8-TO-619R-G
				A6 MISCELLANEOUS PARTS		
				NOTE When repairing the Timing Pod, most of the individual cabinet parts can be ordered and replaced. However, when any part of the cable assembly is damaged, the whole Timing Pod and Cable assembly must be replaced. Order HP Part Number 05005-60102, which includes all the parts shown in Figure 6-5.		
	05005-60102	0	1	CABLE ASSEMBLY-POD	28480	05005-60102
MP26	05005-40008	3	1	BOOT-POD CABLE	28480	05005-40008
MP37	7120-8785	7	1	LABEL POD-TOP	28480	7120-8785
MP38	05005-40001	6	2	COVER-POD	28480	05005-40001
MP39	7120-8784	6	1	LABEL POD-BOTTOM	28480	7120-8784
MP40	05005-40010	7	1	BOOT-POD	28480	05005-40010
MP41	05005-40011	8	1	BOOT-POD LEADS	28480	05005-40011
MP42	05005-00005	6	1	SHIELD-POD	28480	05005-00005
MP43	05005-00006	7	1	INSULATOR-POD	28480	05005-00006
A6W2	05005-60112	2		CABLE ASSEMBLY-START/ST-SP, WG	28480	05005-60112
A6W3	05005-60113	3		CABLE ASSEMBLY-STOP/QUAL, W/R	28480	05005-60113
A6W4	05005-60114	4		CABLE ASSEMBLY-CLK, W/Y	28480	05005-60114
A6W5	05005-60115	5		CABLE ASSEMBLY-GND, BLACK	28480	05005-60115
A7	0960-0444	2	1	LINE MODULE-UNFILTERED	28480	0960-0444
A7C1A/B	0160-0676	6	1	CAPACITOR-FXD 1800PF/1800PF ±10%	28480	0160-0676
A7F1	2110-0202	1	1	FUSE .5A 250V TD 1.25 X .25 UL	75915	313.500
A7F1 (Alternate)	2110-0201	0	1	FUSE -.25 AT 250V TD 1.25 X .25 UL (FOR 240V OPERATION)	75915	313.250

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts List (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
				MISCELLANEOUS PARTS		
B1	0950-1589	7	1	FAN-TBAX 48-CFM 6-16VDC/WITH MOTOR CONTROL	28480	0950-1589
T1	9100-0465	4	1	TRANSFORMER-POWER 100/120/220/240V	28480	9100-0465
W1	8120-1521	6	1	CABLE ASSY 18AWG 3-CNDCT JGK-JKT	28480	8120-1521
W2	05005-60101	9	1	CABLE ASSEMBLY-POWER	28480	05005-60101
W3	05005-60104	2	1	CABLE ASSEMBLY-60 PIN RB	28480	05005-60104
W4	05005-60116		1	CABLE, PROBE GROUND	28480	05005-60116
				MISCELLANEOUS/CHASSIS PARTS		
MP2	4040-1541	6	1	SHELL-BOTTOM	28480	4040-1541
MP1	4040-1542	7	1	SHELL-TOP	28480	4040-1542
MP23	7101-0518	8	1	PANEL-FRONT	28480	7101-0518
MP11	7120-5370	0	2	LABEL-HANDLE	28480	7120-5370
MP10	7120-8782	4	1	LABEL-NAMEPLATE (5005A)	28480	7120-8782
MP30	7120-8787	9	1	LABEL-5V CONNECTOR (5005A)	28480	7120-8787
MP29	7120-8788	0	1	LABEL-POWER (5005A)	28480	7120-8788
MP6	5040-7223	4	2	FOOT-BOTTOM SHELL	28480	5040-7223
MP7	5040-8044	9	4	SPACER, BLACK PLASTIC	28480	5040-8044
	5041-0243	6	7	KEY CAP-UNLIGHTED	28480	5041-0243
	5041-0252	7	10	KEY CAP-QUARTER	28480	5041-0252
	5041-1845	6	2	KEY CAP-SPL	28480	5041-1845
MP20	05005-00001	2	1	PANEL-REAR	28480	05005-00001
MP15	05005-00002	3	1	BRACKET-FAN	28480	05005-00002
MP13	05005-00003	4	1	BRACKET-FAN GTS	28480	05005-00003
MP24	05005-40002	7	1	BEZEL	28480	05005-40002
MP4	05005-40003	8	1	COVER-STORAGE	28480	05005-40003
MP3	05005-40005	0	1	HANDLE	28480	05005-40005
MP21	05005-40006	1	2	FOOT-REAR PANEL	28480	05005-40006
MP22	05005-40007	2	1	TRIM STRIP	28480	05005-40007
MP9	10230-62101	7	5	GRABBER	28480	10230-62101

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Manufacturer's Code List

MFR NO.	MANUFACTURER'S NAME	ADDRESS	ZIP CODE
00000	ANY SATISFACTORY SUPPLIER		
01121	ALLEN-BRADLEY CO	MILWAUKEE WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS TX	75222
0192B	RCA CORP SOLID STATE DIV	SOMERVILLE NJ	08876
02111	SPECTROL ELECTRONICS CORP	CITY OF IND CA	91745
02114	FERROXCUBE CORP	SAUGERTIES NY	12477
03508	GE CO SEMICONDUCTOR PROD DEPT	SYRACUSE NY	13201
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX AZ	85062
06665	PRECISION MONOLITHICS INC	SANTA CLARA CA	95050
1F556	PRECISION LAMP INC	MOUNTAIN VIEW CA	94040
11236	CTS OF BERNE INC	BERNE IN	46711
13103	THERMALLOY CO	DALLAS TX	75234
16299	CORNING GL WK ELEC CMPNT DIV	RALEIGH NC	27604
17856	SILICONIX INC	SANTA CLARA CA	95054
19701	MEPCO/ELECTRA CORP	MINERAL WELLS TX	76067
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD PA	16701
25088	SIEMENS CORP	ISELIN NJ	08830
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA CA	95051
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO CA	94304
32293	INTERSIL INC	CUPERTINO	95014
34335	ADVANCED MICRO DEVICES INC	SUNNYVALE CA	94086
34344	MOTOROLA INC	FRANKLIN PARK IL	60131
34649	INTEL CORP	MOUNTAIN VIEW CA	95051
52763	STETTNER–TRUSH INC	CAZENOVIA NY	13035
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS MA	01247
72136	ELECTRO MOTIVE CORP SUB IEC	WILLIMANTIC CT	06226
75915	LITTELFUSE INC	DES PLAINES IL	60016
98291	SEALECTRO CORP	MAMARONECK NY	10544

SECTION VII
MANUAL CHANGES

7-1. INTRODUCTION

7-2. This section contains information necessary to adapt this manual to apply to older instruments.

7-3. MANUAL CHANGES

7-4. This manual applies directly to Model 5005A Signature Multimeters with serial number prefix 2112A.

7-5. As engineering changes are made, newer instruments may have serial prefix numbers higher than 2112A. The manuals for these instruments will be supplied with yellow "MANUAL CHANGE" sheets, containing the required information. Replace affected pages or modify existing manual information as directed in the "MANUAL CHANGE" pages. Contact the nearest Hewlett-Packard Sales and Service Office if the change information is missing.

7-6. OLDER INSTRUMENTS

7-7. If your instrument's serial number prefix is lower than 2112A, perform the backdating that applies to your instruments serial prefix, as listed in *Table 7-1* below.

Table 7-1. Manual Backdating

If Instrument has Serial Prefix	Make the Following Changes to the Manual
2108A	1
1952A	1,2
1932A	1,2,3

CHANGE 1 (2108A)

Page 6-7, *Table 6-2,* A3 Replaceable Parts:
Change A3 series number from 2112 to 2108.
Change A3U4 from 1818-1542 (ROM) to 05005-80002; CD 1; EPROM-PROGRAMMED; 28480; 05005-80002.
Change A3U11 from 1818-1543 (ROM) to 05005-80003; CD 2; EPROM-PROGRAMMED; 28480; 05005-80003.
Change A3U13 from 1818-1544 (ROM) to 05005-80004; CD 3; EPROM-PROGRAMMED; 28480; 05005-80004.

NOTE

Part Numbers 05005-80002, 05005-80003, and 5005-80004 are no longer available. If replacement is necessary, order part numbers 1818-1542, 1818-1543, and 1818-1544.

CHANGE 2 (1952A, excluding serial numbers 00247, 249, 250, 252-255, 257-259, 261-285)

Page 6-3, *Table 6-2,* A1 Replaceable Parts:
Change A1 series number from 2108 to 1952.
Change A1C50 from 0160-0573 (4700pf) to 0160-0572; CD 1;
Capacitor-Fxd 2200pf ±20% 100VDC CER; 28480; 0160-0572.

Page 8-97, *Figure 8-21,* A1 Schematic Diagram:
Change series number (top of diagram) from 2108 to 1952.
Change A1C50 from 4700pf to 2200pf.

CHANGE 3 (1932A)

Page 6-7, *Table 6-2,* A3 Replaceable Parts:
Change A3 series number from 1952 to 1932.
Delete XS1, XS2; 1200-0607; Socket - IC 16-cont.

SECTION VIII
SERVICE

8-1. INTRODUCTION

8-2. This section contains the information needed to service the HP Model 5005A. The information includes theory of operation, recommended test equipment, schematic diagram notes, safety considerations, assembly/disassembly procedures, troubleshooting information, and block and schematic diagrams. This section also includes a cross-reference table, *Table 8-1*, to aid the correlation of assembly reference designations with their HP part numbers.

8-3. THEORY OF OPERATION

8-4. The theory of operation is presented in three stages:

- General Instrument Description. These paragraphs present an overview of the operation and capability of the 5005A. This dicussion references the Simplified Block Diagram in *Figure 8-13.*
- Block Diagram Description. These paragraphs describe the various Measurement Techniques and all Function Modes, and reference the Detailed Block Diagram in *Figure 8-20.*
- Detailed Circuit Theory. These paragraphs arranged by assembly order, describe the individual circuits at the component level, and reference the individual assembly schematic diagrams.

8-5. The schematic diagrams for all of the assemblies are located at the end of this section. They are arranged in numerical order according to the assembly number (i.e., A1, A2, A3, etc.) in *Figure 8-21* through *8-25.*

8-6. TROUBLESHOOTING

8-7. Troubleshooting for the 5005A is presented through a series of troubleshooting procedures. Many of the procedures utilize the built-in Diagnostics, designed to exercise and verify critical circuits using signature analysis, signal tracing, and conventional measurements. These procedures can efficiently isolate malfunctions to component level for diagnosis. Troubleshooting is keyed to the Overall Troubleshooting Flowchart in *Figure 8-14.*

8-8. RECOMMENDED TEST EQUIPMENT

8-9. Test equipment and test equipment accessories required to maintain the 5005A are listed in *Table 1-2.* Equipment other than that listed may be used if it meets the listed critical specifications. The following paragraphs describe additional equipment whose use is optional, but can prove very helpful during troubleshooting.

8-10. HP 545A Logic Probe, HP 546A Logic Pulser, and HP 547A Current Tracer.

8-11. The Logic Probe, Logic Pulser, and Current Tracer are self contained troubleshooting instruments designed to stimulate and measure digital activity in logic circuits. When bad signatures on a Signature Analyzer indicate printed circuit board opens or shorts, these instruments are very effective in isolating the specific point.

8-12. The Logic Probe is self-contained, easy-to-use tool for examining logic nodes. Continuity, signal flow, bus device, address decoder, clock, and switch activity of the 5005A may be verified. The circuits operating characteristics while in defined diagnostic loops may be examined.

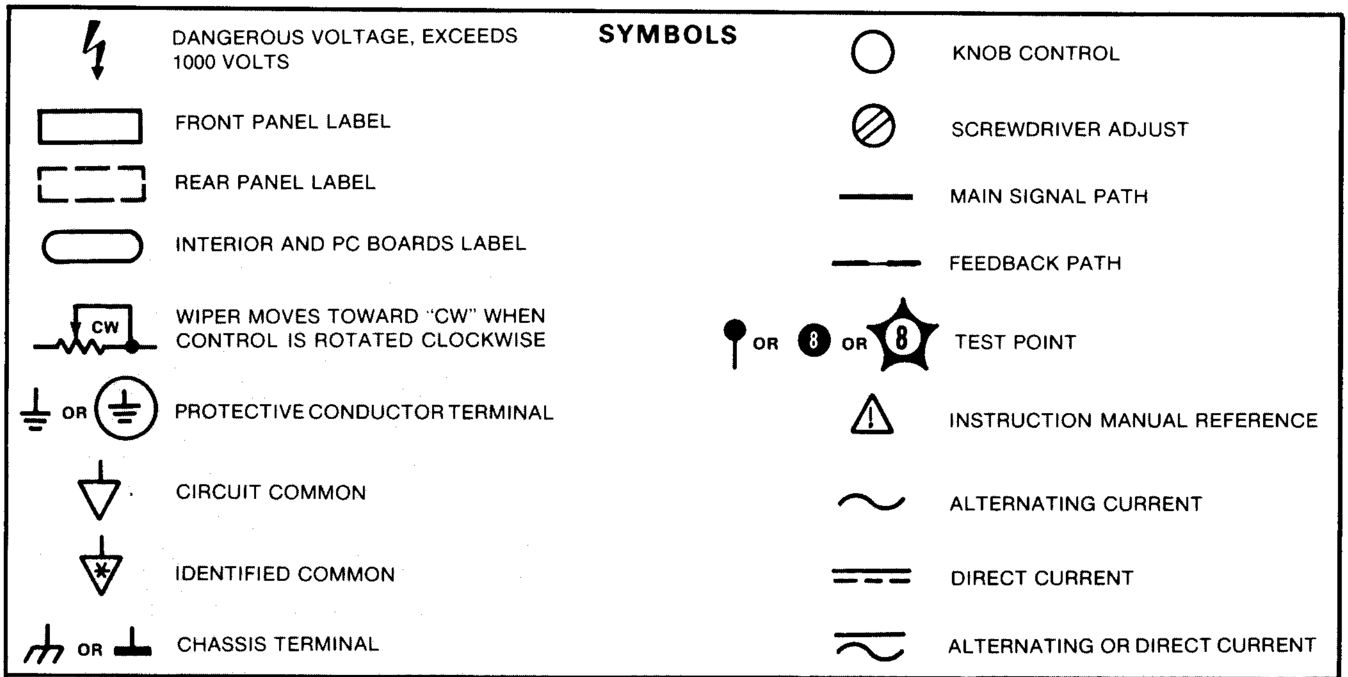
8-13. The Logic Pulser forces overriding pulses into nodes. It can be programmed to output single pulses, pulse streams, or bursts. The pulser can be used to force ICs to enable or clock. When used with the Logic Probe, logic circuit inputs can be pulsed while their outputs are monitored with the probe. By this means, correct signal propagation through logic elements can be verified.

8-14. The Current Tracer can be used to monitor current activity on a logic node or power bus, and can tell approximately how much pulse current is present and what path it takes. When a Logic Pulser is used to inject current into a nonactive (no pulse activity) node, the impedance and the nature of possible stuck nodes (e.g., output, hard short) can be estimated. Then the actual low impedance point can be found by tracing the path of the current from the Logic Pulser to the location where the current either goes to a short or enters a component.

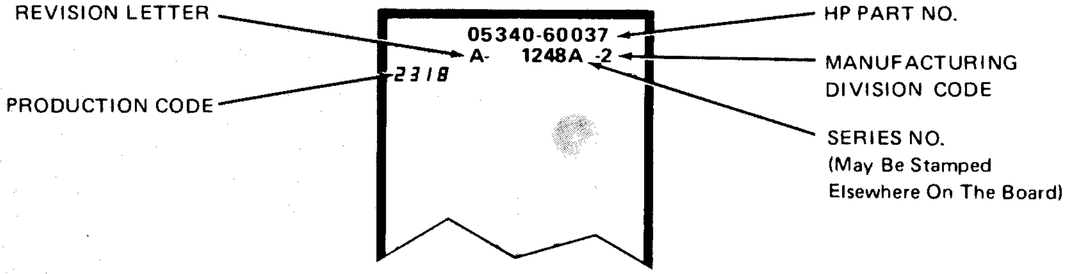
8-15. SCHEMATIC DIAGRAM SYMBOLS AND REFERENCE DESIGNATORS

8-16. *Figure 8-1* shows the symbols used on the schematic diagrams. At the bottom of *Figure 8-1*, the system for reference designators, assemblies, and subassemblies is shown.

SYMBOLS


DANGEROUS VOLTAGE, EXCEEDS 1000 VOLTS
FRONT PANEL LABEL
REAR PANEL LABEL
INTERIOR AND PC BOARDS LABEL
CW
WIPER MOVES TOWARD "CW" WHEN CONTROL IS ROTATED CLOCKWISE
OR
PROTECTIVE CONDUCTOR TERMINAL
CIRCUIT COMMON
IDENTIFIED COMMON
OR
CHASSIS TERMINAL
KNOB CONTROL
SCREWDRIVER ADJUST
MAIN SIGNAL PATH
FEEDBACK PATH
OR
8
OR
8
TEST POINT
INSTRUCTION MANUAL REFERENCE
ALTERNATING CURRENT
DIRECT CURRENT
ALTERNATING OR DIRECT CURRENT

PRINTED CIRCUIT BOARD IDENTIFICATION


REVISION LETTER
PRODUCTION CODE
05340-60037
A-
1248A
-2
2318
HP PART NO.
MANUFACTURING DIVISION CODE
SERIES NO.
(May Be Stamped Elsewhere On The Board)

REFERENCE DESIGNATIONS

REFERENCE DESIGNATIONS WITHIN ASSEMBLIES ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION. JACKS ARE THE STATIONARY CONNECTORS AND PLUGS ARE THE MORE MOVEABLE OF TWO CONNECTORS.

ASSEMBLY	ABBREVIATION	COMPLETE DESCRIPTION
A25	C1	A25C1
A25A1	CR1	A25A1CR1
NO PREFIX	J3	J3

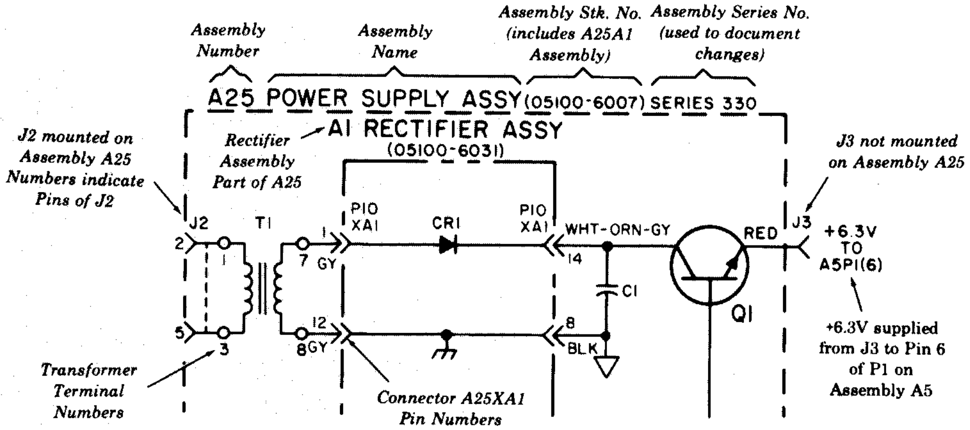

Assembly Number
Assembly Name
Assembly Stk. No. (includes A25A1 Assembly)
Assembly Series No. (used to document changes)
A25 POWER SUPPLY ASSY (05100-6007) SERIES 330
J2 mounted on Assembly A25 Numbers indicate Pins of J2
Rectifier Assembly Part of A25
A1 RECTIFIER ASSY
(05100-6031)
J3 not mounted on Assembly A25
J2
T1
P10
XA1
CR1
P10
XA1
WHT-ORN-GY
RED
J3
+6.3V TO A5P1(6)
2
1
7 GY
14
C1
Q1
5
3
12
8GY
8
BLK
Transformer Terminal Numbers
Connector A25XA1 Pin Numbers
+6.3V supplied from J3 to Pin 6 of P1 on Assembly A5

Figure 8-1. Schematic Diagrams Notes

8-17. ASSEMBLY DESIGNATIONS

8-18. Assemblies such as printed circuit boards are assigned numbers in sequence, A1, A2, etc., as shown in *Table 8-1*. As shown in *Figure 8-1*, subassemblies within an assembly are given a subordinate A number. For example, rectifier subassembly A1, has the complete designator A25A1. For individual components, the complete designator is determined by adding the assembly number and subassembly number, if any. For example, CR1 on the rectifier assembly is designated A25A1CR1.

Table 8-1. Assembly Identification

ASSEMBLY	DESCRIPTION	HP PART NUMBER
A1	Main Assembly	05005-60001
A2	DVM Assembly	05005-60002
A3	Microprocessor and Display Drive Assembly	05005-60003
A4	Display and Keyboard Assembly	05005-60004
A5	Data Probe Assembly	05005-60005
A6	Timing Pod Assembly	05005-60006
A7	Line Module Assembly	0960-0444

8-19. Identification Markings on Printed Circuit Boards

8-20. HP printed circuit boards (see *Figure 8-1*) have four verification numbers; an assembly part number, a series number, a revision letter, and a production code. The assembly part number has 10 digits (such as 05359-60021) and is the primary identification. All assemblies with the same part number are interchangeable. When a production change is made on an assembly that makes it incompatible with previous assemblies, a change in part number is required. The series number (such as 1748) is used to document minor electrical changes. As changes are made, the series number is incremented. When replacement boards are ordered, you may receive a replacement with a different series number. If there is a difference between the series number marked on the board and the schematic in this manual, a minor electrical difference exists. If the number on the printed circuit board is lower than that on the schematic, refer to Section VII for backdating information. If it is higher, refer to the yellow looseleaf manual sheets for this manual. If the manual change sheets are missing, contact your local HP Sales and Service Office. See the listing on the back cover of this manual.

8-21. Revision letters (A, B, etc.) denote changes in printed circuit layout. For example, if a capacitor type is changed (electrical value may remain the same) and requires different spacing for its leads, the printed circuit board layout is changed and the revision letter is incremented to the next letter. When a revision letter changes, the series number is also usually changed. The production code is the four-digit, seven-segment number used for production purposes.

8-22. SAFETY CONSIDERATIONS

8-23. Although the 5005A has been designed in accordance with international standards, this manual contains information, caution, and warnings which must be followed to ensure safe operation and to retain the 5005A in safe operating condition. Service and adjustments should be performed only by qualified service personnel.

WARNING

ANY INTERRUPTION OF THE PROTECTIVE (GROUNDING) CONDUCTOR (INSIDE OR OUTSIDE THE 5005A) OR DISCONNECTION OF THE PROTECTIVE EARTH TERMINAL IS LIKELY TO MAKE THE 5005A DANGEROUS.

8-24. Any adjustment, maintenance, and repair of the opened 5005A under voltage should be avoided as much as possible and, when inevitable, should be carried out only by skilled personnel who are aware of the hazard involved. Capacitors inside the 5005A may still be charged even if the 5005A has been disconnected from its source of power.

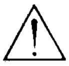
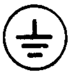
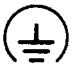
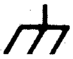
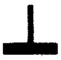
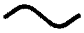
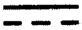
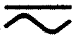
8-25. Make sure that only fuses with the required rated current and of the specified type (normal blow, time delay, etc.) are used for replacement. The use of repaired fuses and the short circuiting of fuseholders must be avoided. Whenever it is likely that this protection has been impaired, the 5005A must be made inoperative and be secured against any unintended operation.

WARNING

THE SERVICE INFORMATION IS OFTEN USED WITH POWER SUPPLIED AND PROTECTIVE COVERS REMOVED FROM THE 5005A. ENERGY AVAILABLE AT MANY POINTS MAY, IF CONTACTED, RESULT IN PERSONAL INJURY.

8-26. Safety Symbols

8-27. The following safety symbols are used on the instrument front panel, printed-circuit boards, and in the manuals:

	Instruction manual symbol. The product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the instrument.
OR 	Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.
	Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. A terminal marked with the symbol must be connected to ground in the manner described in the installation (operating) manual, before operating the equipment.
 OR 	Frame and chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.
	Alternating current (power line).
	Direct current (power line).
	Alternating or direct current (power line).
WARNING	The WARNING signal denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury.
CAUTION	The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

8-28. SERVICE AIDS

8-29. *Pozidriv Screwdrivers.* Many screws in the 5005A appear to be Phillips type, but are not. To avoid damage to the screw slots, Pozidriv screwdrivers should be used.

8-30. *Service Aids on Printed Circuit Boards.* The servicing aids on the printed circuit boards include test points, reference designators, adjustment callouts, and assembly stock numbers.

8-31. *Diagnostic Routines.* The 5005A provides a selection of user designated self diagnostic routines, which are permanently stored in ROM. These utilize interactive instrument testing with both conventional measurement techniques and digital Signature Analysis. The technician should have an understanding of the concepts of Signature Analysis as an in-circuit troubleshooting technique. Hewlett-Packard makes available a variety of Application Notes on the concepts and useage of Signature Analysis. It may be helpful to contact the nearest Hewlett-Packard Sales and Service Office (offices are listed at the back of this manual) and request a copy of the Signature Analysis publications index:

*AN INDEX TO SIGNATURE ANALYSIS PUBLICATIONS, Application Note 222-0.

8-32. LOGIC SYMBOLS

8-33. Logic symbols used in this manual conform to the American National Standard ANSI Y32.14-1973 (IEEE Std. 91-1973). This standard supersedes MIL-STD-806B. In the following paragraphs logic symbols are described. For further descriptions refer to HP Logic Symbology manual, part number 5951-6116.

8-34 Logic Concepts

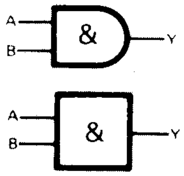
8-35. The binary numbers 1 and 0 are used in pure logic where 1 represents true, yes, or active and 0 represents false, no, inactive. These terms should not be confused with the physical quantity (e.g., voltage) that may be used to implement the logic, nor should the term "active" be confused with a level that turns a device on or off. A truth table for a relationship in logic shows (implicitly or explicitly) all the combinations of true and false input conditions and the result (output). There are only two basic logic relationships, AND and OR. The following illustrations assume two inputs (A and B), but these can be generalized to apply to more than two inputs.

AND Y is true if and only if A is true and B is true (or more generally, if all inputs are true).
Y=1 if and only if A=1 **and** B=1
Y=A•B

TRUTH TABLE

A	B	Y
1	1	1
1	0	0
0	1	0
0	0	0

EQUIVALENT SYMBOLS

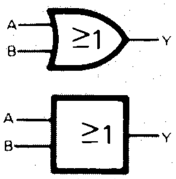


OR Y is true if and only if A is true or B is true (or more generally, if one or more input(s) is (are) true).
Y=1 if and only if A=1 **or** B=1
Y=A+B

TRUTH TABLE

A	B	Y
1	1	1
1	0	1
0	1	1
0	0	0

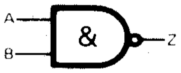
EQUIVALENT SYMBOLS



8-36. Negation

8-37. In logic symbology, the presence of the negation indication symbol ○ provides for the presentation of logic function inputs and outputs in terms *independent* of their physical values, the 0-state of the input or output being the 1-state of the symbol referred to the symbol description.

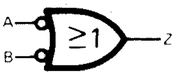
EXAMPLE 1



TRUTH TABLE

A	B	Z
1	1	0
1	0	1
0	1	1
0	0	1

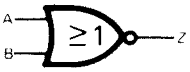
EXAMPLE 2



TRUTH TABLE

A	B	Z
1	1	0
1	0	1
0	1	1
0	0	1

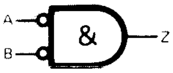
EXAMPLE 3



TRUTH TABLE

A	B	Z
1	1	0
1	0	0
0	1	0
0	0	1

EXAMPLE 4



TRUTH TABLE

A	B	Z
1	1	0
1	0	0
0	1	0
0	0	1

EXAMPLE 1 says that Z is *not* true if A is true *and* B is true or that Z is true if A *and* B are *not* both true. $\overline{Z}=AB$ or $Z=\overline{AB}$. This is frequently referred to as NAND (for NOT AND).

EXAMPLE 2 says that Z is true if A is *not* true *or* if B is *not* true. $Z=\overline{A}+\overline{B}$. Note that this truth table is identical to that of Example 1. The logic equation is merely a DeMorgan's transformation of the equations in Example 1. The symbols are equivalent.

EXAMPLE 3 $\overline{Z}=A+B$ or $Z=\overline{A+B}$ and,

EXAMPLE 4 $Z=\overline{A}\bullet\overline{B}$, also share common truth table and are equivalent transformations of each other. The NOT OR form (Example 3) is frequently referred to as NOR.

NOTE

In this manual the logic negation symbol is NOT used.

8-38. Logic Implementation and Polarity Indication

8-39. Devices that can perform the basic logic functions, AND and OR, are called gates. Any device that can perform one of these functions can also be used to perform the other if the relationship of the input and output voltage levels to the logic variables 1 and 0 is redefined suitably.

8-40. In describing the operation of electronic logic devices, the symbol H is used to represent a "high level", which is a voltage within the more-positive (less-negative) of the two ranges of voltages used to represent the binary variables. L is used to represent a "low level", which is a voltage within the less-positive (more-negative) range.

8-41. A function table for a device shows (implicitly or explicitly) all the combinations of input conditions and the resulting output conditions.

8-42. In graphic symbols, inputs or outputs that are active when at the high level are shown without polarity indication. The polarity indicator symbol ◺ denotes that the active (one) state of an input or output *with respect to the symbol to which it is attached* is the low level.

NOTE

The polarity indicator symbol " ◺ " is used in this manual.

EXAMPLE 5 assume two devices having the following function tables.

DEVICE #1
FUNCTION TABLE

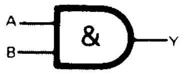
A	B	Y
H	H	H
H	L	L
L	H	L
L	L	L

DEVICE #2
FUNCTION TABLE

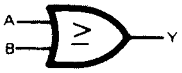
A	B	Y
H	H	H
H	L	H
L	H	H
L	L	L

POSITIVE LOGIC by assigning the relationship H=1, L=0 at both input and output, Device #1 can perform the AND function and Device #2 can perform the OR function. Such a consistent assignment is referred to as positive logic. The corresponding logic symbols would be:

DEVICE #1

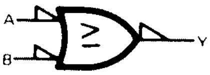


DEVICE #2

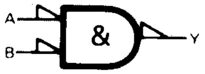


NEGATIVE LOGIC alternatively, by assigning the relationship H=0, L=1 at both input and output, Device #1 can perform the OR function and Device #2 can perform the AND function. Such a consistent assignment is referred to as negative logic. The corresponding logic symbols would be:

DEVICE #1



DEVICE #2

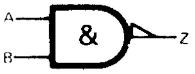


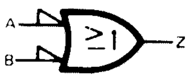
8-43. MIXED LOGIC. The use of the polarity indicator symbol (◺) automatically invokes a mixed-logic convention. That is, positive logic is used at the inputs and outputs that do not have polarity indicators, negative logic is used at the inputs and outputs that have polarity indicators.

EXAMPLE 6
FUNCTION TABLE

A	B	Z
H	H	L
H	L	H
L	H	H
L	L	H

This may be shown either of two ways:



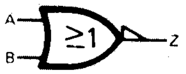


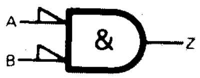
Note the equivalence of these symbols to examples 1 and 2 and the fact that the function table is a positive-logic translation (H=1, L=0) of the NAND truth table, and also note that the function table is the negative-logic translation (H=0, L=1) of the NOR truth table, given in Example 3.

EXAMPLE 7
FUNCTION TABLE

A	B	Z
H	H	L
H	L	L
L	H	L
L	L	H

This may be shown either of two ways:

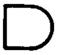
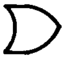




Note the equivalence of these symbols to examples 3 and 4 and the fact that the function table is a positive-logic translation (H=1, L=0) of the NOR truth table, and also note that the function table is the negative-logic translation (H=0, L=1) of the the NAND truth table, given in Example 1.

8-44. It should be noted that one can easily convert from the symbology of positive-logic merely by substituting a polarity indicator (◺) for each negative indicator (**o**) while leaving the distinctive shape alone. To convert from the symbology of negative-logic, a polarity indication (◺) is substituted for each negation indicator (**o**) and the OR shape is substituted for the AND shape or vice versa.

8-45. It was shown that any device that can perform OR logic can also perform AND logic and vice versa. DeMorgan's transformation is illustrated in Example 1 through 7. The rules of the transformation are:

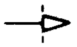
1. At each input or output having a negation (**o**) or polarity (◺) indicator, delete the indicator.
2. At each input or output not having an indicator, add a negation (**o**) or polarity (◺) indicator.
3. Substitute the AND symbol  for the OR symbol  or vice versa.

   These steps do not alter the assumed convention; positive-logic stays positive, negative-logic stays negative, and mixed-logic stays mixed.

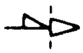
8-46. The choice of symbol may be influenced by these considerations: (1) The operation being performed may best be understood as AND or OR. (2) In a function more complex than a basic gate, the inputs will usually be considered as inherently active high or active low (e.g., the J and K inputs of a J-K flip-flop are active high and active low, respectively). (3) In a chain of logic, understanding and the writing of logic equations are often facilitated if active low or negated outputs feed into active low or negated inputs.

8-47. Other Symbols

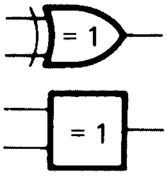
8-48. Additional symbols are required to depict complex logic diagrams, as follows:



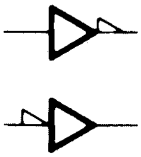
Dynamic input activated by transition from a low level to a high level. The opposite transition has no effect at the output.



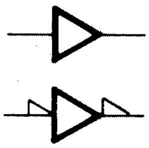
Dynamic input activated by transition from a high level to a low level. The opposite transition has no effect at the output.



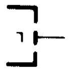
Exclusive OR function. The output will assume its indicated active level if and only if one and only one of the two inputs assumes its indicated active level.



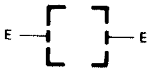
Inverting function. The output is low if the input is high and it is high if the input is low. The two symbols shown are equivalent.



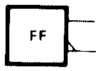
Noninverting function. The output is high if the input is high and it is low if the input is low. The two symbols shown are equivalent.



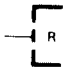
OUTPUT DELAY. The output signal is effective when the input signal returns to its opposite state.



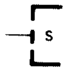
EXTENDER. Indicates when a logic function increases (extends) the number of inputs to another logic function.



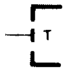
FLIP-FLOP. A binary sequential element with two stable states: a set (1) state and a reset (0) state. Outputs are shown in the 1 state when the flip-flop is set. In the reset state the outputs will be opposite to the set state.



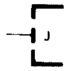
RESET. A 1 input will reset the flip-flop. A return to 0 will cause no further effect.



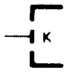
SET. A 1 input will set the flip-flop. A return to 0 will cause no further action.



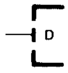
TOGGLE. A 1 input will cause the flip-flop to change state. A return to 0 will cause no further action.



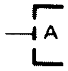
J INPUT. Similar to the S input except if both J and K (see below) are at 1, the flip-flop changes state.



K INPUT. Similar to the R input (see above).



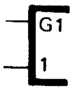
D INPUT (Data). Always dependent on another input (usually C). When the C and D inputs are at 1, the flip-flop will be set. When the C is 1 and the D is 0, the flip-flop will reset.



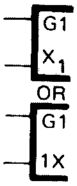
Address symbol has multiplexing relationship at inputs and demultiplexing relationship at outputs.

8-49. Dependency Notation "C" "G" "V" "F"

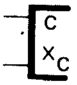
8-50. Dependency notation is a way to simplify symbols for complex IC elements by defining the existence of an AND relationship between inputs, or by the AND conditioning of an output by an input without actually showing all the elements and interconnections involved. The following examples use the letter "C" for control and "G" for gate. The dependent input is labeled with a number that is either prefixed (e.g., 1X) or subscripted (e.g., X_1). They both mean the same thing. The letter "V" is used to indicate an OR relationship between inputs or between inputs and outputs with this letter (V). The letter "F" indicates a connect-disconnect relationship. If the "F" (free dependency) inputs or outputs are active (1) the other usual normal conditions apply. If one or more of the "F" inputs are inactive (0), the related "F" output is disconnected from its normal output condition (it floats).



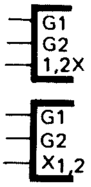
The input that controls or gates other inputs is labeled with a "C" or a "G", followed by an identifying number. The controlled or gated input or output is labeled with the same number. In this example, "1" is controlled by "G1".



When the controlled or gated input or output already has a functional label (X is used here), that label will be prefixed or subscripted by the identifying number.



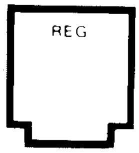
If a particular device has only one gating or control input then the identifying number may be eliminated and the relationship shown with a subscript.



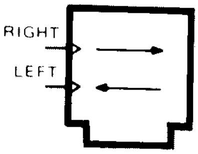
If the input or output is affected by more than one gate or control input, then the identifying numbers of each gate or control input will appear in the prefix or subscript, separated by commas. In this example "X" is controlled by "G1" and "G2".

8-51. Control Blocks

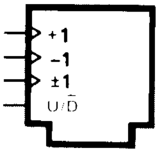
8-52. A class of symbols for complex logic are called control blocks. Control blocks are used to show where common control signals are applied to a group of functionally separate units. Examples of types of control blocks follow.



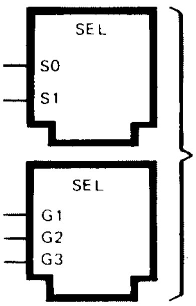
Register control block. This symbol is used with an associated array of flip-flop symbols to provide a point of placement for common function lines, such as a common clear.



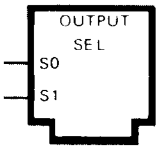
Shift register control block. These symbols are used with any array of flip-flop symbols to form a shift register. An active transition at the inputs causes left or right shifting as indicated.



Counter control block. The symbol is used with an array of flip-flops or other circuits serving as a binary or decade counter. An active transition at the +1 or -1 input causes the counter to increment one count upward or downward, respectively. An active transition at the +1 input causes the counter to increment one count upward or downward depending on the input at an up/down control.



Selector control block. These symbols are used with an array of OR symbols to provide a point of placement for selection (S) or gating (G) lines. The selection lines enable the input desingated 0, 1, ...n of each OR function by means of a binary code where S0 is the least significant digit. If the 1 level of these lines if low, polarity indicators (◺) will be used. The gating lines have an AND relation with the respective input of each OR function: G1 with the inputs numbered 1, G2 with the input numbered 2, and so forth. If the enabling levels of these lines is low, polarity indicators (◺) will be used.



Output selector control block. This symbol is used with a block symbol having multiple outputs to form a decoder. The selection lines enable the output designated 0, 1, ...n of each block by means of a binary code where S0 is the least significant digit. If the 1 level of these lines is low, polarity indicators (◺) will be used.

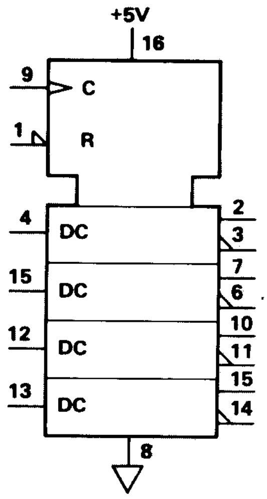
8-53. Complex Logic Devices

8-54. Logic elements can be combined to produce very complex devices that can perform more difficult functions. A control block symbol can be used to simplify understanding of many complex devices. Several examples of complex devices are given here. These examples are typical of the symbols used in schematic diagrams in this manual.

Description:

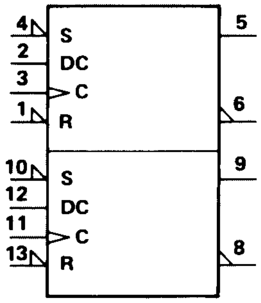
QUAD D-TYPE FLIP-FLOPS

Data at the DC inputs is transferred to the outputs on the positive-going edge of the clock pulse (pin 9). A low signal at the reset (pin 1) will clear all FFs.



Description:

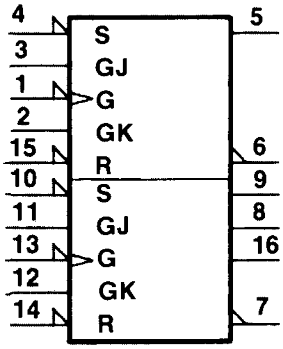
DUAL D-TYPE FLIP-FLOP



The dual D-type flip-flop consists of two independent D-type flip-flops. The information present at the data (D_c)input is transferred to the active-high and active-low outputs on a low-to-high transition of the clock (C) input. The data input is then locked out and the outputs do not change again until the next low-to-high transition of the clock input. The set (S) and reset (R) inputs override all other input conditions: when (S) is low, the active-high output is forced high; when reset (R) is low, the active-high output is forced low. Although normally the active-low output is the complement of the active-high output, simultaneous low inputs at the set and reset will force both the active-low and active-high outputs to go high at the same time on some D-type flip-flops. This condition will exist only for the length of time that both set and reset inputs are held low. The flip-flop will return to some indeterminate state when both the set and reset inputs are returned to the high state.

Description:

DUAL J-K FLIP-FLOPS with Clear and Preset

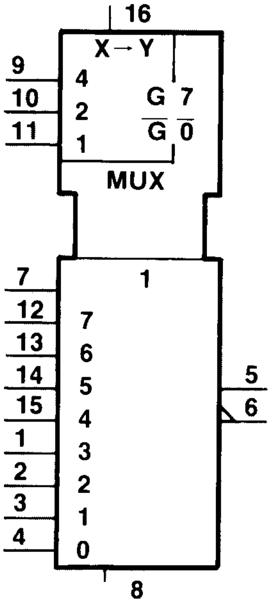


The dual J-K flip-flop consists of two independent J-K type flip-flops. The flip-flop response is determined by the states of GJ and GK inputs, at the instant that a low-going transition is applied to the G input. When GJ and GK are low, the outputs will not change state. When GJ is low and GK is high, the Q output (pin 5 or 9) will go low (unless it is already low). When GJ is high and GK is low, the Q output (pin 5 or 9) will go high (unless it is already high). When GJ and GK are both high, the output will change state with each negative going edge transition at G. The S set and R reset inputs override all other input conditions: when S is low, Q is forced high; when R is low, Q is forced low. The $\overline{Q}$ output (pin 6 or 7) operates as the complement of the Q output (pin 5 or 9).

Description:

DATA SELECTOR/MULTIPLEXER

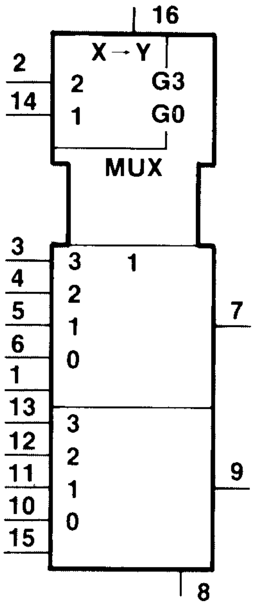
This data multiplexer selects one of eight line inputs, directing it and its complement to the output when enabled. Pins 11, 10, and 9 are the binary weighted "1", "2", and "4" select inputs, respectively. A low on the enable (pin 7) will direct the selected input line data to the output (pin 5). An inverted output of the selected input line data is provided at pin 6.


16
X→Y
9
10
11
4
2
1
G 7
G 0
MUX
7
12
13
14
15
1
2
3
4
1
7
6
5
4
3
2
1
0
5
6
8

Description:

DUAL 4 LINE-TO-1 LINE DATA SELECTOR/MULTIPLEXERS

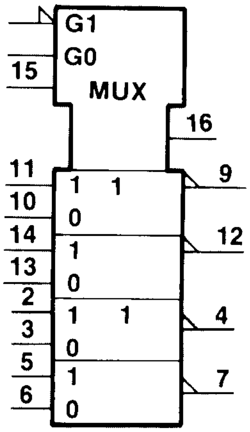
This dual four input multiplexer selects one of four line inputs directing it to the output when enabled. Pins 14 and 2 are the binary weighted "1" and "2" select inputs, respectively. A low on the enable (pin 1 or 15 or both) will direct the selected input line data to the respective output.

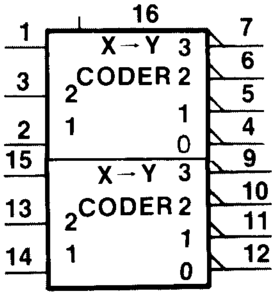

16
X→Y
2
14
2
1
G3
G0
MUX
3
4
5
6
1
13
12
11
10
15
3
2
1
0
1
3
2
1
0
7
9
8

Description:

QUAD 2-LINE-TO-1 LINE DATA SELECTOR/MULTIPLEXERS

This quad two input multiplexer selects one of two word inputs directing it to the output when enabled. The level at G1/G0 (pin 1) selects the input line for all four selectors; a high selects input "0", a low selects input "1". The selected inputs are inverted and directed to their respective outputs unless inhibit line (pin 15) is high. When inhibit (pin 15) is high, all outputs go high.

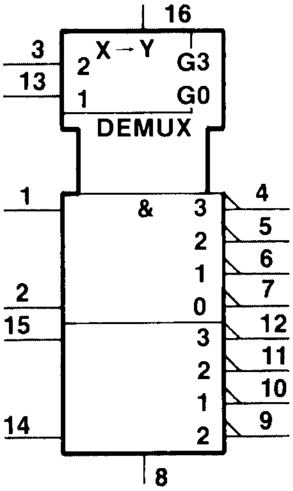

G1
G0
15
MUX
16
11
10
14
13
2
3
5
6
1
0
1
0
1
0
1
0
1
1
9
12
4
7


16
1
3
2
15
13
14
X→Y
CODER
2
1
3
2
1
0
7
6
5
4
9
10
11
12

Description:

DUAL DECODER/DEMULTIPLEXERS

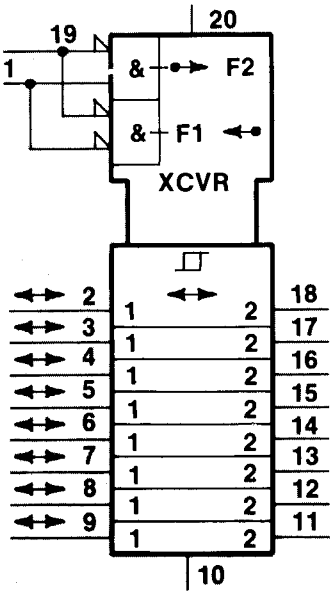
This device consists of two independent two-line to four-line decoders. Pins 2 (14) and 3 (13) are the binary weighted "1" and "2" select lines, respectively. The selected output is forced low, unless the inhibit (pin 1 or 15) is high. When the inhibit is high, all respective decoder outputs go high.


16
3
13
2
1
X→Y
G3
G0
DEMUX
1
2
15
14
&
3
2
1
0
4
5
6
7
12
11
10
9
8

Description:

DUAL 2-LINE-TO-4 LINE DECODER/DEMULTIPLEXERS

This device consists of two separate two-line to four-line decoders, with common select lines. Pins 13 and 3 are the binary weighted "1" and "2" select lines, respectively. The output selected is forced low on both decoder halves. All other outputs are high.


20
19
1
&
F2
&
F1
XCVR
1
2
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
10

Description:

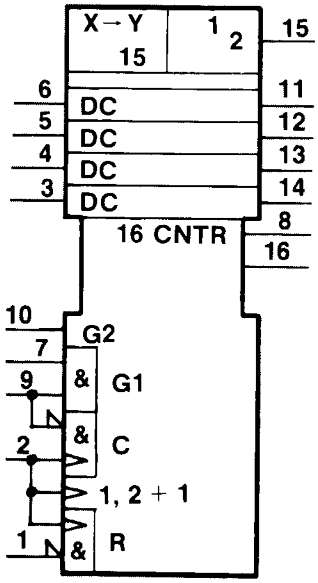
OCTAL BUS TRANSCEIVERS with 3-STATE Outputs

This octal transceiver is an eight-line bi-directional bus transceiver with 3-State outputs. The direction of data transfer is determined by pin 1; a high directs the data from the "1" bus to the "2" bus if enabled, a low directs the data from the "2" bus to the "1" bus if enabled. Pin 19 is the enable. When pin 19 is low, data transfer is enabled in the selected direction. When pin 19 is high, data transfer is disabled and both output buses are set to the high impedance state.

Description:

SYNCHRONOUS 4-BIT COUNTER

This synchronous presettable counter has four master slave flip-flops that are triggered on the positive-going edge of the clock pulse (pin 2). A LOW at the load input (pin 9) disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels at the enable inputs (pins 7 and 10). The clear function (pin 1) is synchronous and a low level at the clear input sets all outputs low after the next clock pulse, regardless of the levels of the enable inputs. Both count enable inputs (pins 7 and 10) must be HIGH to count, and the input T (pin 10) is fed forward to enable the carry output (pin 15).



8-55. REPAIR TECHNIQUES

8-56. Handling and Cleaning of the A2 DVM Assembly.

8-57. The A2 DVM assembly is a high impedance printed circuit board. Areas of the printed circuit board are highly susceptible to contamination from dirt and oils when handled. It is recommended that the A2 DVM assembly be handled ONLY by the edges. Avoid contact with the printed circuit areas, **especially the area around K1, K2, U3, and U4,** with bare fingers. If the printed circuit board surface is contaminated, the DVM may operate in a nonlinear fashion. If this occurs, clean the assembly before attempting to replace components, just to be sure.

8-58. The A2 assembly should be cleaned whenever repairs are completed, or contamination is suspected. The following steps describe the recommended procedure for the repair and cleaning of a high impedance printed circuit board.

a. When replacing components, ALWAYS use a water soluable acid core solder (e.g. HP #8090-0736).

b. Hand wash the printed circuit board, using distilled water, powdered detergent, and a small non-metallic brush. Rinse with distilled water, removing as much soap residue as possible.

CAUTION

Assembly mounted switches and potentiometers may be damaged by cleaning. Remove these types of components if mounted in sockets. Re-lubricate any of these components which are cycled through a cleaning procedure.

c. Next, auto wash using an automatic wash machine, or home type dishwasher. Add dishwasher detergent and cycle.

d. After washing, bake the assembly in a hot chamber or home oven for 24 hours, at 50 degree C (~150 degree F). This is to remove all remaining moisture.

e. After baking and preferably while still warm, spray both sides of the assembly with a light coat of clean, clear plastic type protectant coating. This seals the assembly from moisture and humidity.

NOTE

High impedance printed circuit boards can also be cleaned with a high quality solvent or degreaser, such as FREON TF® (HP Part #8500-0232). Never use a cleaner that contains oils or that leaves a residue. Spray or brush lightly, then rinse with isopropyl alcohol, blow dry with compressed air, bake for 24 hours, and spray coat as described above. Note, however, that this type of cleaning will remove the protectant coating applied at the factory. Always re-coat the assembly with a plastic type protective spray whenever a solvent or degreaser is used to clean.

8-59. Removal of Assembly Plastic Hinges

8-60. The A1, A2, and A3 assemblies are connected together by interlocking black plactic hinges. Two hinges are mounted to each assembly, pressed into alignment slots and secured with a small drop of super adhesive.

8-61. The hinges are not normally intended to be removed. Should one become cracked or broken, it can be removed and replaced. To remove, heat the damaged part with a heat gun (hair dryer), occasionally rocking back and forth, until it loosens. Pull the part straight off, away from the board edge. Place a drop of adhesive near the PC board slot, and quickly install the new part. Be sure to properly position the new hinge before mounting. The posts should always point to the left, while looking at the J1 sixty pin connector edge of the assembly.

8-62. Disassembly and Reassembly

8-63. The following procedures are divided into two catagories; Main Cabinet Disassembly and PC Board Removal. The Main Cabinet Disassembly procedures open the instrument and, utilizing the hinged PC board feature, allow serviceable access to all the assemblies within the HP 5005A, under normal power-up conditions. Following this, the PC Board Removal procedures describe how to disassemble and remove each of the individual assemblies from the instrument. Reassembly is essentially the reverse of the disassembly procedures.

8-64. The following tools are required for these procedures:

1. Large Pozidriv screwdriver.
2. Small Pozidriv screwdriver.
3. Small flat-bladed screwdriver.
4. Needle-nose pliers.

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8-65. Before performing any of the following disassembly or reassembly procedures:

a. Set LINE switch to OFF.

b. Remove the line power cable from the rear panel power module.

WARNING

LINE VOLTAGE IS EXPOSED WITHIN THE 5005A EVEN WHEN THE LINE SWITCH IS SET TO OFF. REMOVAL OF THE POWER CORD IS NECESSARY TO FULLY UNPOWER THE 5005A.

8-66. MAIN CABINET DISASSEMBLY

a. Removal of the front Storage Cover. Pull gently at the pivot points of the handle, spreading it slightly, and swing it out of the way of the front Storage Cover. Open the cover and remove the Data Probe and Timing Pod assemblies. Remove the front Storage Cover from the instrument by bending the spring retainer together, freeing the hinge points. See *Figure 8-2*.

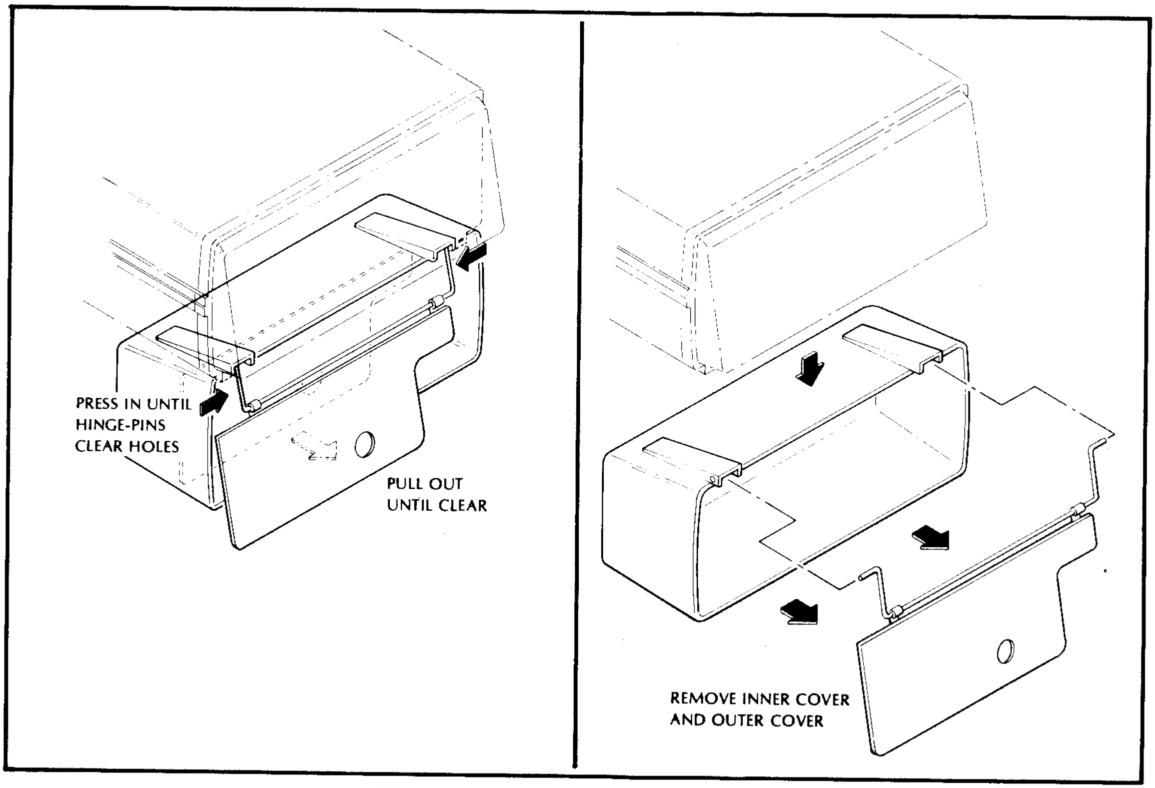

PRESS IN UNTIL HINGE-PINS CLEAR HOLES
PULL OUT UNTIL CLEAR
REMOVE INNER COVER AND OUTER COVER

Figure 8-2. Storage Cover Removal

b. Removal of the top cover. Turn the instrument upside-down and remove the four pozidriv screws recessed in the bottom cover. Turn the instrument back over and remove the top cover.

c. Removal of spacers. There are four black spacers, shaped like tubes, approximately 5 cms (2.0 inches) long, in each corner. Remove all four, retaining one to be used as a tool in following steps.

d. Removal of the bottom cover. The instrument is secured to the bottom cover with two pozidriv screws, located at the center and rear edge center of the A1 Main Assembly. See *Figure 8-3.* Remove the screw at the rear edge center.

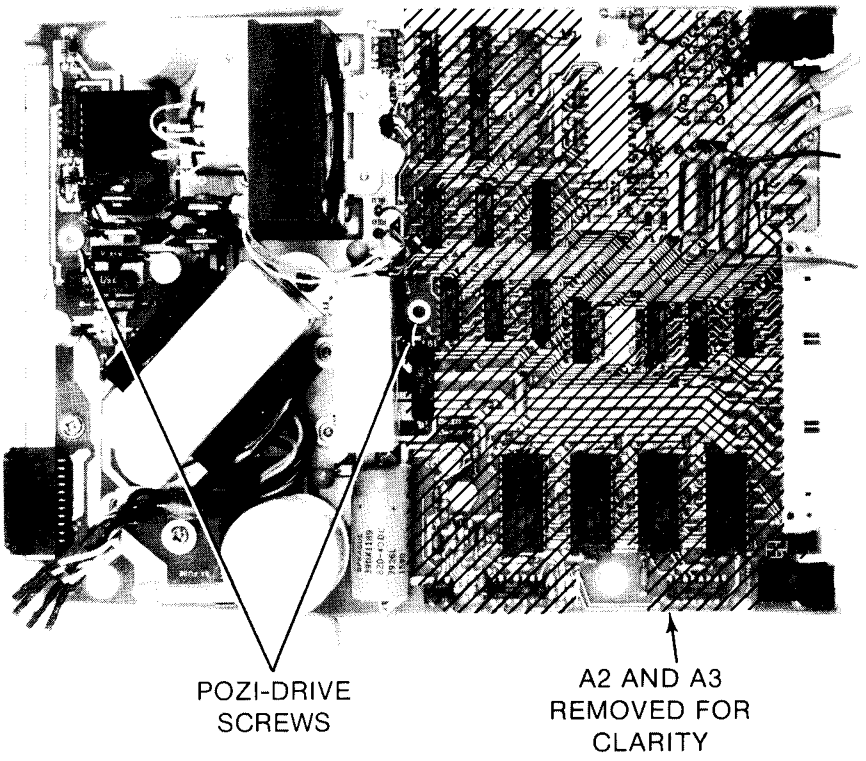


Figure 8-3. Bottom Cover Removal

In order to remove the screw at the center of A1, the top PC board, A3 Microprocessor Assembly, must be raised slightly. The top two circuit boards in the instrument are hinged for ease of service. Do not remove them from the hinge unless necessary. There are two white plastic standoffs near the rear of each of the top two circuit boards. These standoffs have locks to hold the hinged boards in place during normal use.

To unlock the printed circuit board from the standoff, take the black tube spacer (from previous step) and place the small hole in the end, over the top of the standoff. Press firmly while applying slight upward pressure on the board near the standoff. See *Figure 8-4.* Repeat for the other standoff.

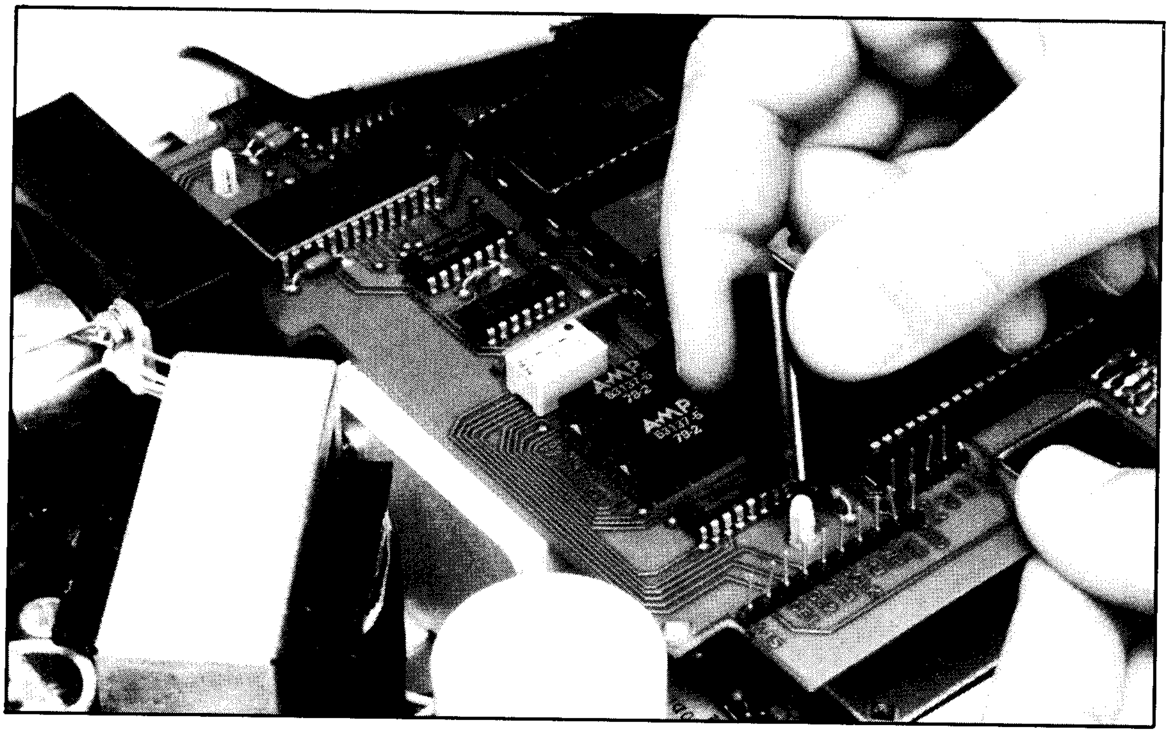


Figure 8-4. Locking Standoff Release

Raise the A3 Microprocessor assembly about 45 degrees, just enough to access the pozidriv screw in the center of A1. See *Figure 8-5*. Do not raise the A3 assembly higher, do not force the board. Remove the center screw and reseat the A3 Assembly. Lift straight up on the rear panel legs and front panel, and remove the complete instrument from the bottom cover. Holding the instrument in a horizontal position, rotate it 90 degrees and rest it on the bottom cover.

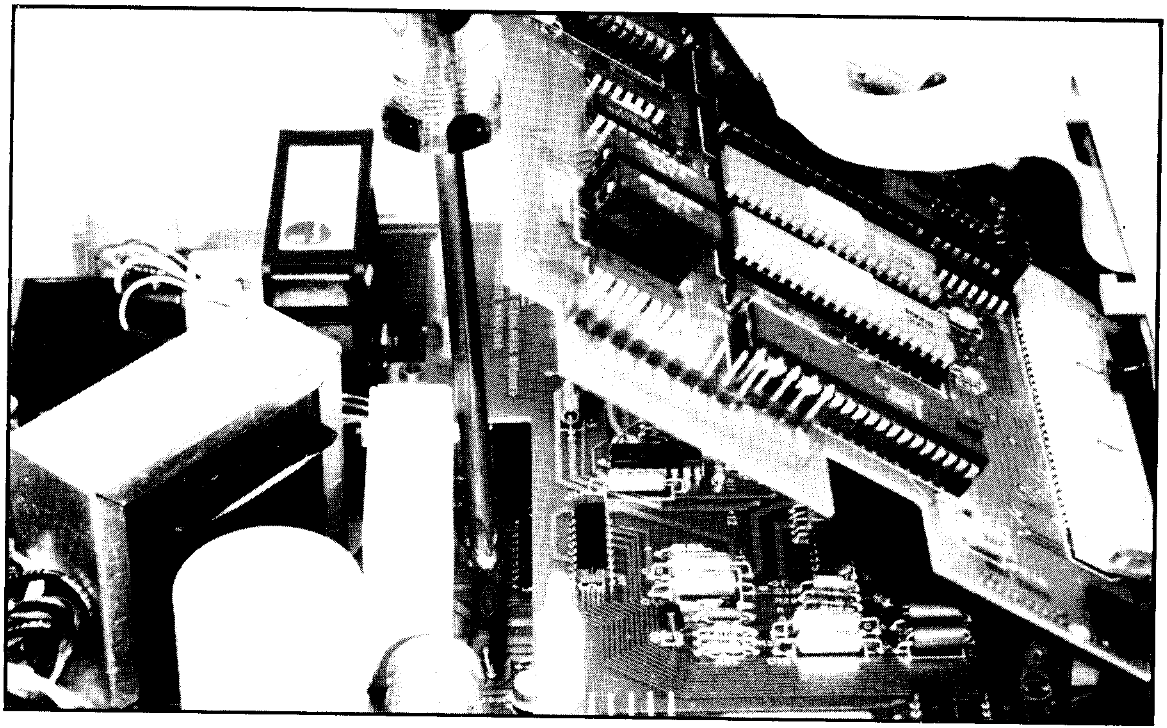


Figure 8-5. Accessing Center Screw

e. Repositioning of the front panel housing. For better access to the various assemblies, the front panel housing of the instrument can be repositioned. Using needle-nose pliers, remove the two retaining springs holding the front panel housing to the main instrument. Disconnect the 34 line flat ribbon cable from the right side of the A3 Microprocessor Assembly. Slide the housing straight forward, off the PC board guides, while feeding the Data Probe and Timing Pod cables carefully through the front panel cable boots. See *Figure 8-6*. Replace the flat ribbon cable.

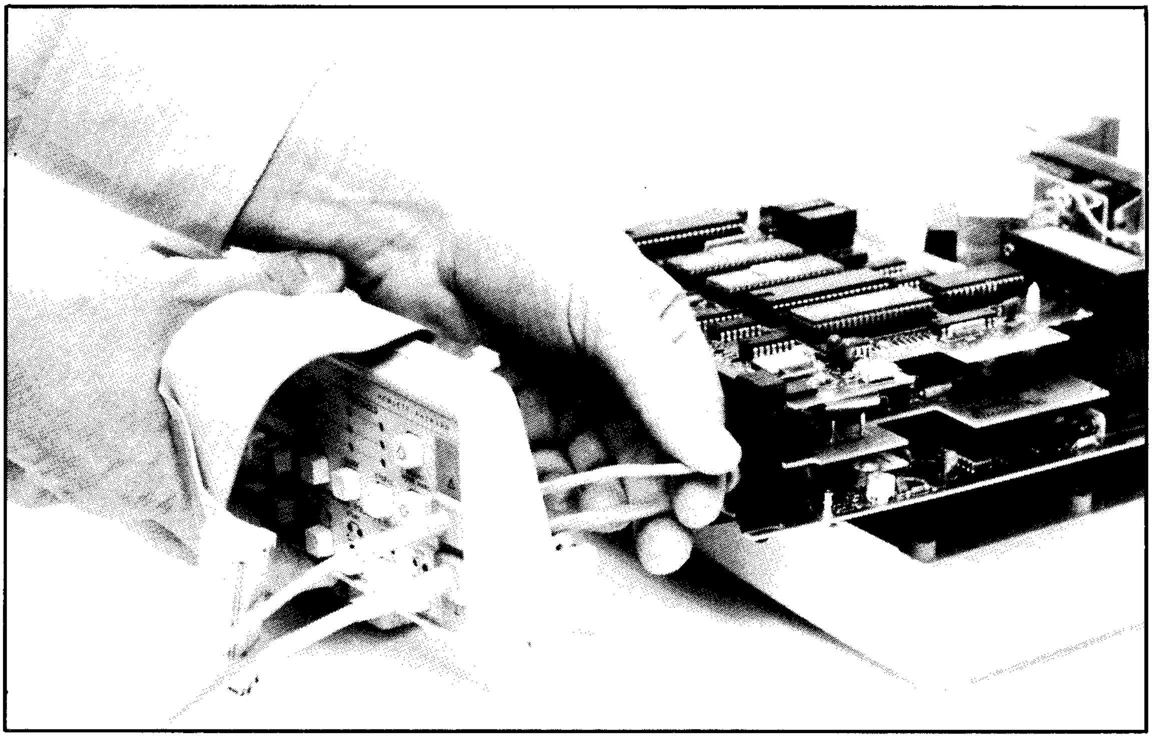


Figure 8-6. Reposition Front Panel

f. Raising hinged assemblies. Unlock the top PC board, A3 Microprocessor Assembly, as described in step d, and raise it about 90 degrees. This exposes the middle board, A2 DVM, for service or adjustment. Note that no cables have to be removed and the instrument will continue to function if power is applied.

WARNING

THE A2 DVM PRINTED CIRCUIT BOARD IS A HIGH IMPEDANCE PC BOARD. IT IS EXTREMELY SENSITIVE TO CONTAMINATION FROM DIRT AND OILS, APPLIED WHEN HANDLING WITH BARE HANDS. CONTAMINATION CAN CAUSE DRIFT, NONLINEARITY, OR INOPERATION. DO NOT HANDLE THE A2 DVM ASSEMBLY WITH BARE FINGERS, EXCEPT AT THE EDGES.

Using the black tube, release the locks on the middle board standoffs, and raise the A2 DVM assembly up on its hinge, about 90 degrees. The A3 Microprocessor assembly will continue traveling to a horizontal position. At this time, the A3, A2, and A1 Assemblies are all accessible, and if power is applied, the instrument can be operated normally. See *Figure 8-7.*

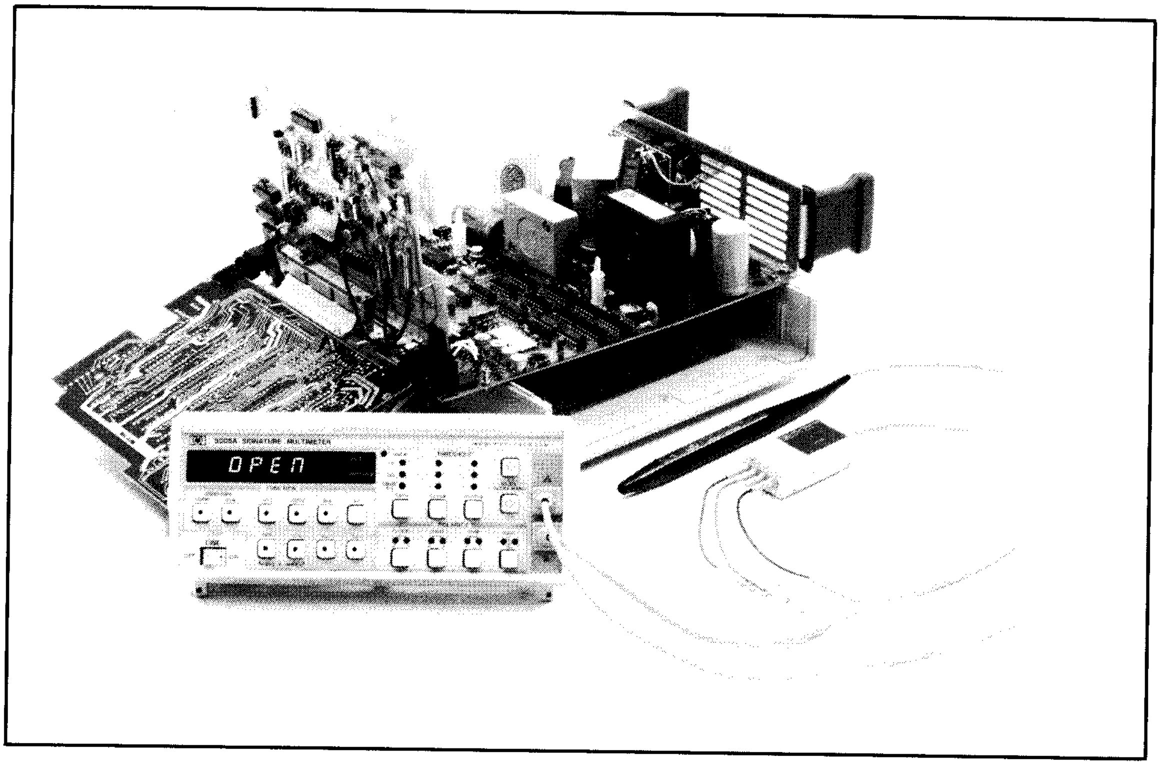


Figure 8-7. Open and Operating

8-67. PC BOARD REMOVAL

8-68. Before performing any of the following disassembly or reassembly procedures:

a. Set LINE switch to OFF.

b. Remove the line power cable from the rear panel power module.

8-69. To remove the individual printed circuit board assemblies, first perform steps a. through e., then proceed as follows:

WARNING

LINE VOLTAGE IS EXPOSED WITHIN THE 5005A EVEN WHEN THE LINE SWITCH IS SET TO OFF. REMOVAL OF THE POWER CORD IS NECESSARY TO FULLY UNPOWER THE 5005A.

8-70. A4 Display Assembly Removal

8-71. Removal of the A4 Display Assembly first requires removal of the Front Panel from the front panel housing. Disconnect the edge connector on the 34 line flat ribbon cable at the right side of the A3 Microprocessor assembly. Slide the front panel assembly forward, carefully feeding the Data Probe and Timing Pod cables through the boots. Remove the trim strip at the top of the Front Panel. This is accomplished by using a small flat-bladed screwdriver to release the three trim strip retainers, located on the inside top of the front panel housing. See *Figure 8-8.*

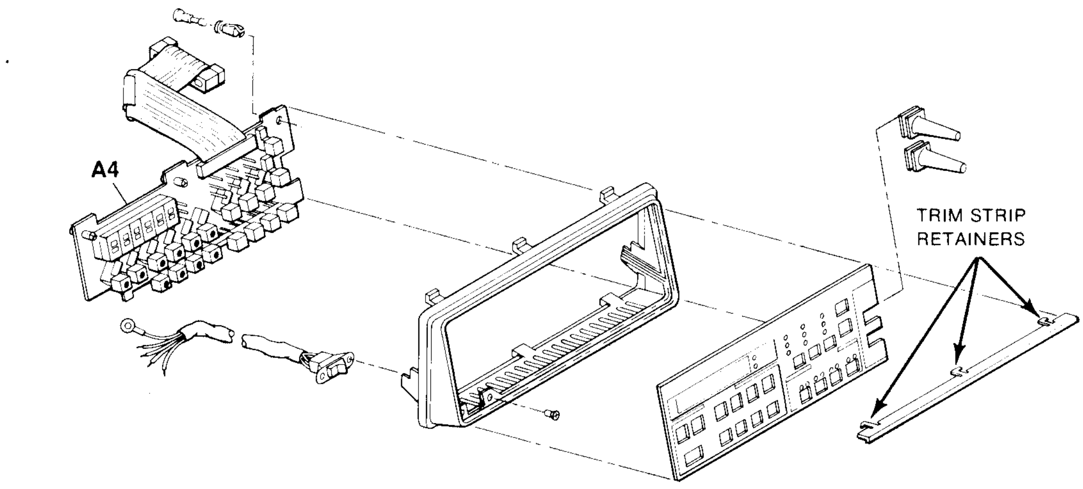


Figure 8-8. Removing A4 Display Assy

8-72. The Front Panel can be removed by tilting the panel forward over its bottom edge, until it clears the LINE switch. The cable boots for the Data Probe and Timing Pod may be removed by sliding them to the right. Note the position of of the cable boots as a reminder for reassembly (i.e. the Data Probe cable is mounted above the Timing Pod cable, and the flat edge of each cable boot is placed to the right, or outside of the front panel). The LINE switch may be removed by removing the two retaining screws. The A4 Display Assembly may now be removed by releasing the three black plunger type fasteners, at the top rear of the assembly, by gently pulling out on each fastener until it reaches its stop. Tilt the assembly back until it is free of the housing.

8-73. A7 Line Module/Rear Panel Disassembly

8-74. The rear panel is removed by removing the three screws on the rear edge of the A1 Main Assembly, and removing the nine push-on wires to the A7 Line Module. Refer to *Figure 8-9,* when replacing the push-on wires during reassembly.

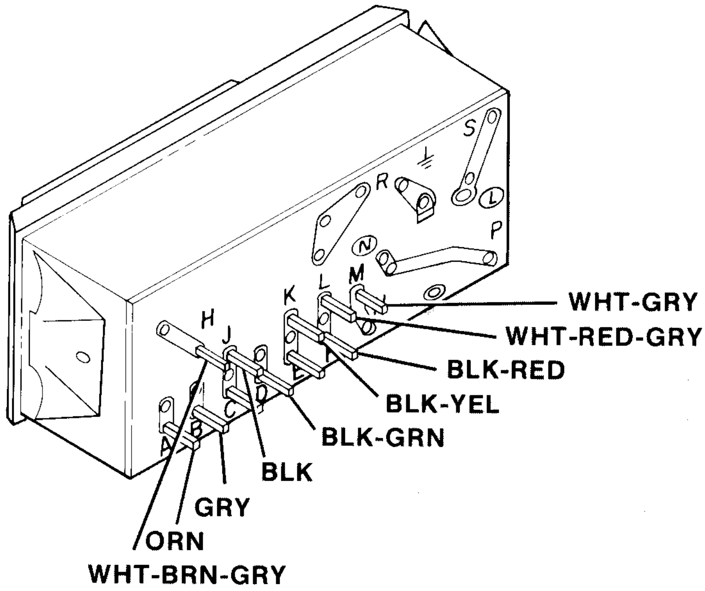
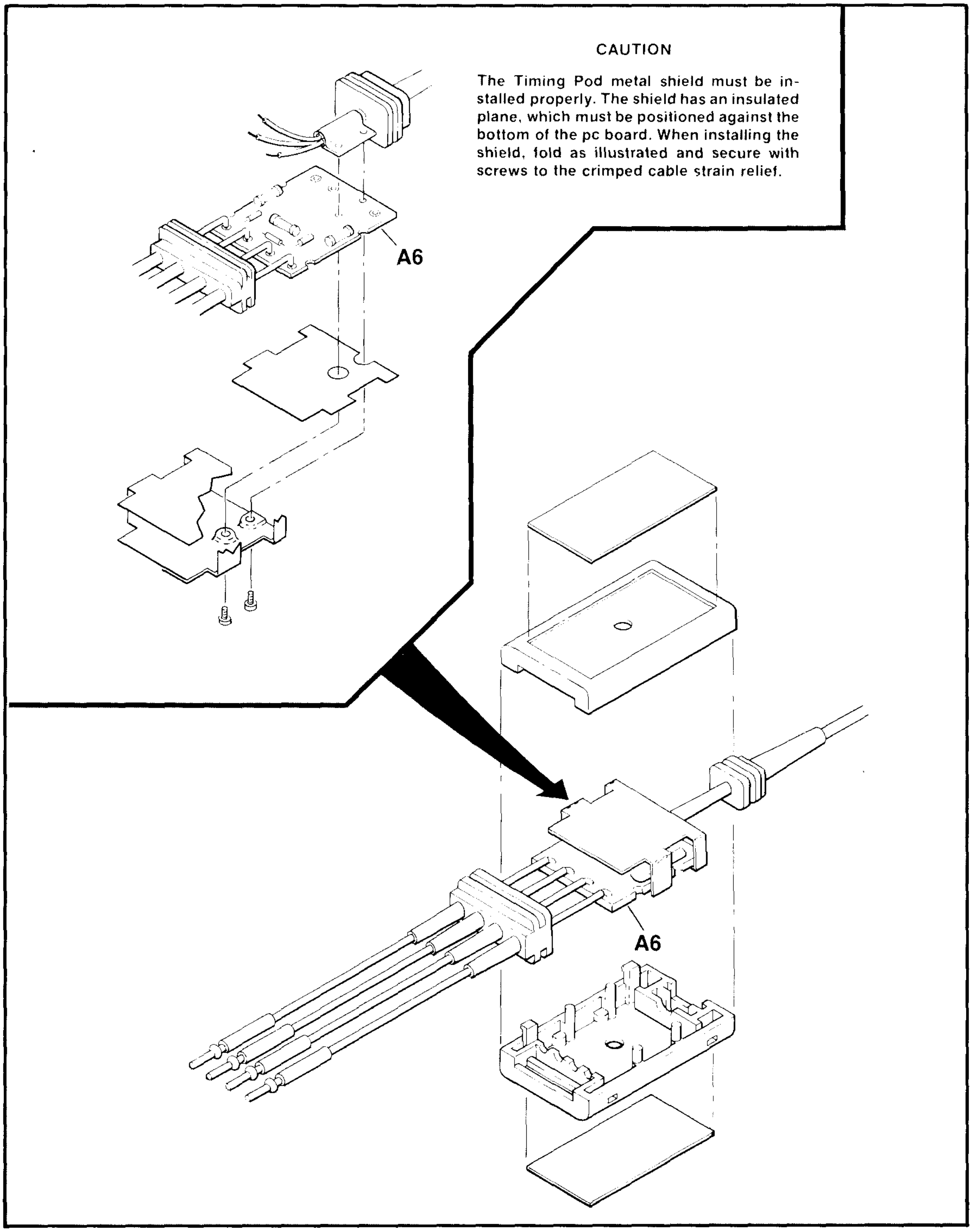

S
R
N
L
P
K
L
M
H
J
A
B
C
D
E
F
WHT-GRY
WHT-RED-GRY
BLK-RED
BLK-YEL
BLK-GRN
BLK
GRY
ORN
WHT-BRN-GRY

Figure 8-9. Line Module Connections

8-75. A6 Timing Pod Disassembly

8-76. The Timing Pod halves are secured together by four locking retainers, two located on either side of the pod. To disassemble the pod, insert the tip of a small flat-bladed screwdriver, pressing in on the retainer, while gently separating the pod halves. Note the positions of the wire colors as a reminder for reassembly; green=ST/SP/START, red=QUAL/STOP, yellow=CLOCK, and black ⊥. The metal shield may be removed by removing the two retaining screws. Note the insulator on the inside of the shield. When reassembling, insure the shield is folded such that the insulator is replaced between the PC board and the shield.



CAUTION

The Timing Pod metal shield must be installed properly. The shield has an insulated plane, which must be positioned against the bottom of the pc board. When installing the shield, fold as illustrated and secure with screws to the crimped cable strain relief.

Figure 8-10. Disassembled Timing Pod

8-77. A5 Data Probe Disassembly

8-78. To disassemble the Data Probe, unscrew the Data Probe tip and pull off the red window. Slide the bottom probe body half off first, (this is the probe body half without the ground pin). Lift the top probe body off, being careful not to bend the ground pin which protrudes slightly through the probe body half. The A5 Data Probe Assembly printed circuit board can be removed from the cable boot by firmly grasping the boot, while gently flexing the the PC board, rocking it side to side, until it clears the stops on the boot. See *Figure 8-11.*

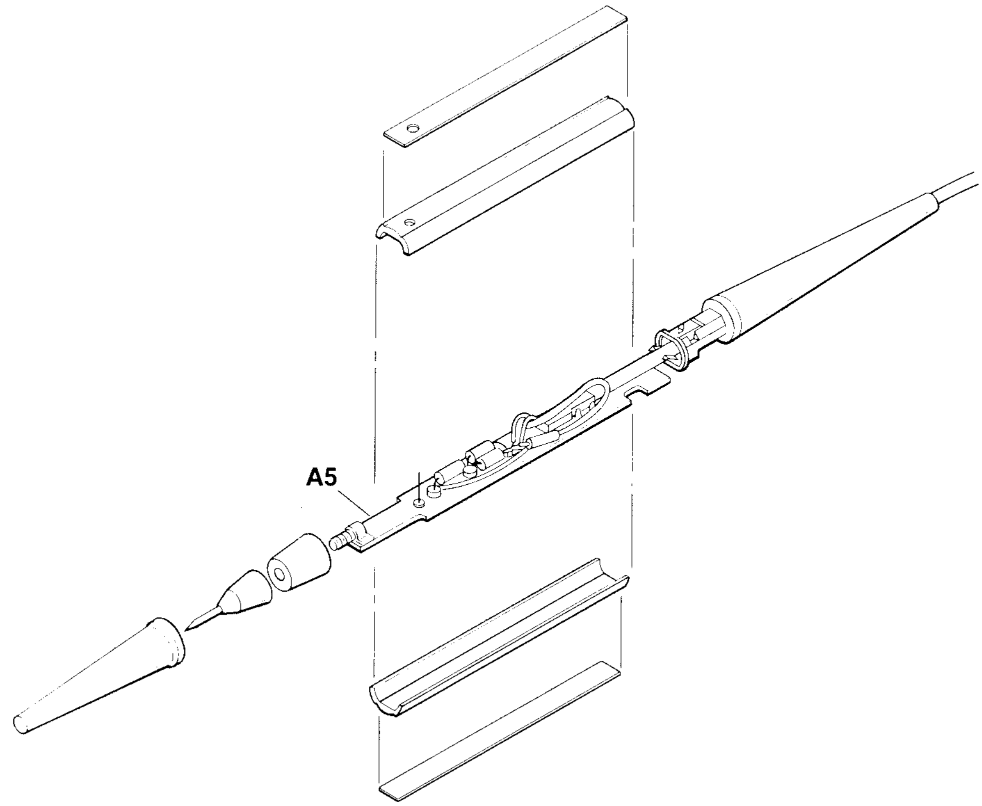


Figure 8-11. Disassembled Data Probe

8-79. A3 Microprocessor Assembly Removal

8-80. To remove the A3 Microprocessor Assembly, disconnect the 60 line ribbon cable located near the front of the instrument. To disconnect this cable, push the ears of the connector (located at each end) outwards until the ribbon cable unseats. Remove the cable completely by hand. The A3 assembly may now be removed by raising the board on the hinges slightly, and sliding to the right. See *Figure 8-12.*

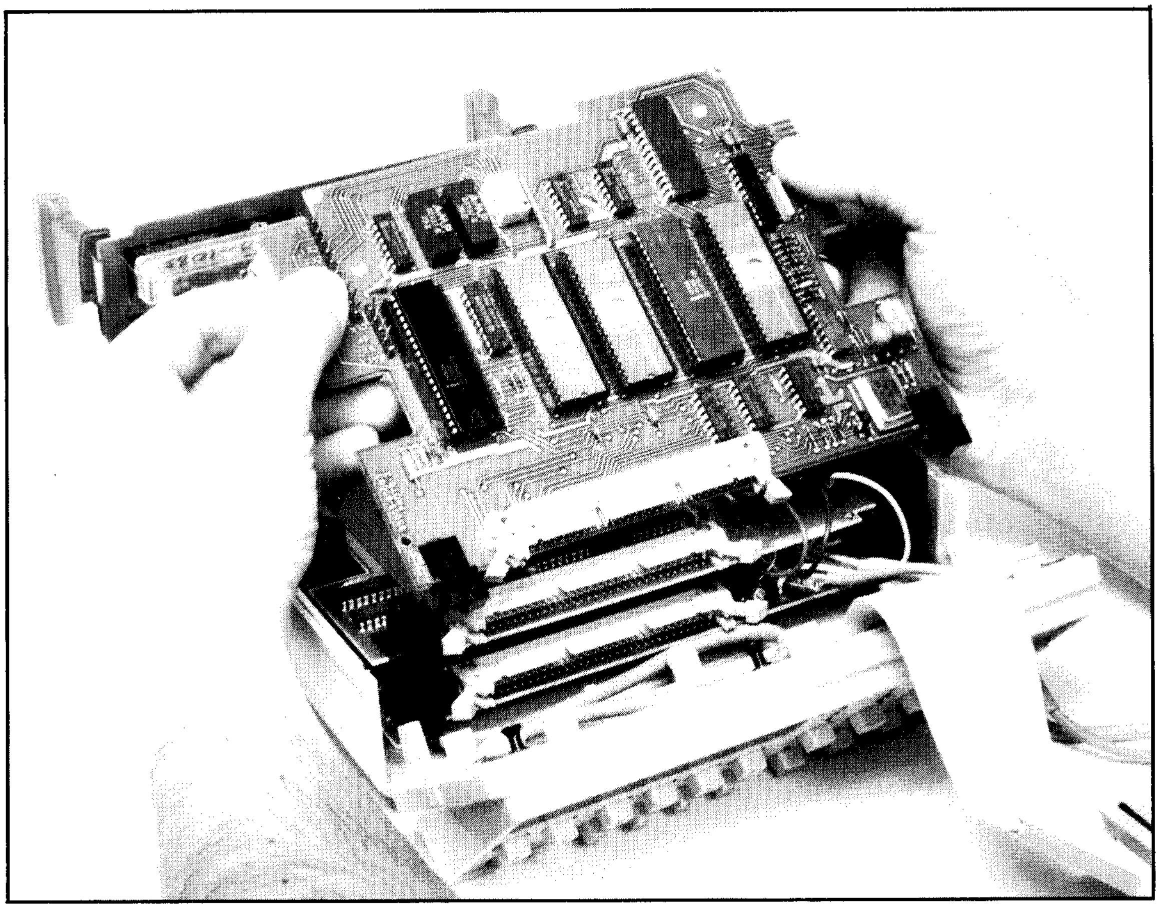


Figure 8-12. Removing A3 Microprocessor Assembly

8-81. A2 DVM Assembly Removal

8-82. To remove the A2 DVM Assembly, first remove the 60 line ribbon cable and A3 Microprocessor Assembly, as described above. Disconnect the three jumper wires (black, red and green) from the gold posts on A2. Note that the jumpers are color-coded, and that the colors are annotated on A2 and A1. The A2 DVM assembly may now be removed by raising the board on the hinges slightly, and sliding to the right.

WARNING

THE A2 DVM PRINTED CIRCUIT BOARD IS A HIGH IMPEDANCE PC BOARD. IT IS EXTREMELY SENSITIVE TO CONTAMINATION FROM DIRT AND OILS, APPLIED WHEN HANDLING WITH BARE HANDS. CONTAMINATION CAN CAUSE DRIFT, NONLINEARITY, OR INOPERATION. DO NOT HANDLE THE A2 DVM ASSEMBLY WITH BARE FINGERS, EXCEPT AT THE EDGES.

8-83. INSTRUMENT REASSEMBLY

8-84. Reassembly procedures are essentially the reverse of the disassembly procedures.

8-85. SIGNAL NAMES

8-86. *Table 8-2* is a list of the signal names used in the 5005A. The list is in alphabetical order, and includes the mnemonic used on the schematic diagram signal. The source, destination, and a description of the function is provided for each signal.

8-87. Ten of the signal lines generated by the A3 Microprocessor Assembly are multiplexed. That is, ten of the lines have two mnemonic names assigned. These lines are routed from the A3 Microprocessor Assembly to two separate locations on the A1 Main Assembly schematic. Both destinations are identified with the same connector pin number, and are electrically the same point.

Table 8-2. Signal Names

SIGNAL	FROM	TO	DESCRIPTION
a - g, dp	A3J2(34,33, 17, 13, 14, 32, 18, 6)	A4	Segment drive lines for A4 Display matrix.
A - D	A3J1 (11, $\overline{12}$, $\overline{13}$, 13)	A2J1	Binary switch address data for A2 Analog Crosspoint Switches. Code defines the switch which will be set to the state of SW, on the next STROBE.
B0 - B3	A2J1 ($\overline{4}$, 1, $\overline{5}$, $\overline{6}$)	A3J1	DVM binary output data. Identifies measurement Bit.
CLK EDGE	A3J2 (26)	A4	Drive line for front panel CLOCK falling edge annunciator LED.
CLK EDGE	A3J2 (27)	A4	Drive line for front panel CLOCK rising edge annunciator LED.
COMBINED START/STOP $\overline{\text{SIGN}}$	A3J1 ($\overline{24}$)	A1J1	Control line for A1 Start/Stop Selector. Control line for selection of polarity A1 DACs. Lo=19, Hi=21.
DV SIGN	A2J1 ($\overline{7}$)	A3J1	DVM output data polarity status bit.
DEVICE ENABLE 0 -7	A3J2 (6, 3, 2, 30, 4, 22, 8, 1, 7)	A4	Column enable lines for A4 Display matrix.
DA0 CLOCK EDGE	A3J1 (25)	A1J1	Input data for A1 DAC Address Decoder. Binary weighted value selects one of four DAC enables. Control line for A1 synchronizer logic. State determines which input Clock edge is used.
DA1 STOP/QUAL EDGE	A3J1 ($\overline{23}$)	A1J1	Input data for A1 DAC Address Decoder. Binary weighted value selects one of four DAC enables. Control line for A1 Edge Selector. State determines which input Stop/Qual edge is used.

Table 8-2. Signal Names (Continued)

SIGNAL	FROM	TO	DESCRIPTION
DATA (PROBE)	A1J1 ($\overline{28}$)	A3J1	Status line for A1 Voltage Comparators. Used to signal comparator transition during offset calibration.
OVOL	A2J1 ($\overline{1}$)	A3J1	Overvoltage. Active high whenever DVM detects an overvoltage input. Flags microprocessor interrupt RST5.5, which isolates the input from the DVM.
$\overline{\text{DSTR}}$	A3J1 (20)	A1J1	Data Strobe. Initiates active low enable to one of four A1 DACs, as defined by address lines DA0, DA1.
D1 - D5	A2J1 (2, $\overline{2}$, $\overline{9}$, $\overline{10}$, $\overline{8}$)	A3J1	DVM binary output data. Represents DVM output digit Data.
END OF MEASURE	A1J1 (30)	A3J1	Status line for A1 Stop Measure flip-flop to the A3 microprocessor.
GATE	A1J1 ($\overline{27}$)	A3J1	Status line from A1 Start Measure flip-flop, through U2B, to the A3 microprocessor.
GATE LIGHT	A3J2 (31)	A4	Level shifted GATE line, used to drive front panel GATE annunciator.
$\overline{\text{K1}}$	A3J1 ($\overline{14}$)	A2J1	Control line for A2 DVM Ohm Control Relay. Low activates relay.
$\overline{\text{K2}}$	A3J1 ($\overline{15}$)	A2J1	Control line for A2 DVM Data/Cal Relay. Low activates relay.
$\overline{\text{K3}}$	A3J1 ($\overline{29}$)	A1J1	Control line for A1 Pull-to-Voltage Relay. Low activates relay.
$\overline{\text{K4}}$	A3J1 ($\overline{30}$)	A1J1	Control line for A1 Data Switch Relay. Low activates relay.
LSB COUNT	A1J1 (29)	A3J1	Least significant bit from A1 counter prescaler U20B. Combines with REGISTER DATA to produce seventeen bits of measurement data.
M/Z	A2J1 ($\overline{3}$)	A3J1	Status line from A2 DVM to A3 microprocessor. Indicates whether the DVM is in Measurement or auto-Zero mode of operation.
$\overline{\text{OUTPUT SHIFT ENABLE}}$	A3J1 ($\overline{22}$)	A1J1	Control line to reset A1 Measure flip-flops, and enable the FSR to serially output measurement data.
$\overline{\text{POP}}$	A3J1 (23)	A1J1	Power on preset, used to initialize A1 synchronizer and tracker flip-flops.
REGISTER DATA	A1J1 (28)	A3J1	MSB of FSR counter. Used to output measurement data, serially to the A3 microprocessor. Sixteen bits are output, one at a time, by DATA STROBE.

Table 8-2. Signal Names (Continued)

SIGNAL	FROM	TO	DESCRIPTION
$\overline{\text{RESET}}$		A2J1	Resets divide-by-61 counters. Used only during factory board test.
$\overline{\text{START MEASURE}}$	A3J1 (24)	A1J1	Control line to reset A1 Start Measure flip-flop.
SYNC	A3J1 (26)	A1J1	Control line for A1 Synchronizer Selector U22B. Used to direct the selection of synchronous or asynchronous inputs to Selectors.
START	A3J1 (3)	A2J1	Control line for A1 microprocessor to A2 DVM. Starts A/D conversion.
STROBE	A3J1 (10)	A2J1	Control line from A1 microprocessor to A2 Analog Crosspoint Switches. High state latches the switch data and address lines in, activating the indicated switch.
SW	A3J1 (12)	A2J1	Control bit from A1 microprocessor to A2 Analog Crosspoint Switches. State defines desired condition of addressed switch.
ST_╱‾EDGE	A3J2 (12)	A4	Drive line for front panel START rising edge annunciator LED.
ST‾╲_EDGE	A3J2 (11)	A4	Drive line for front panel START falling edge annunciator LED.
POLARITY DIFF TD0	A3J1 (27)	A1J1	Control line, used during QUAL S.A. to select either the positive or negative Start edge, as the Stop edge. Threshold DAC input data bit.
TD1	A3J1 ($\overline{26}$)	A1J1	Threshold DAC input data bit.
START EDGE TD2	A3J1 ($\overline{25}$)	A1J1	Control line, used to route either postive or negative Start edge. Threshold DAC input data bit.
DATA STROBE TD3	A3J1 ($\overline{21}$)	A1J1	Control line to shift measurement data, one bit at a time, from the FSR, out REGISTER DATA. Threshold DAC input data bit.
SIGNATURE-TI TD4	A3J1 (22)	A1J1	Control line for A1 Data/Clock Selector. High during S.A. and T. I. function modes. Threshold DAC input data bit.

Table 8-2. *Signal Names (Continued)*

SIGNAL	FROM	TO	DESCRIPTION
COUNT	A3J1 ($\overline{20}$)	A1J1	Control line for A1 Data/Clock Selector. Low only during S.A.
TD5			Threshold DAC input data bit.
FREQ-SIGN	A3J1 (21)	A1J1	Control line for A1 Start/Stop Selector. High during S.A. and frequency function modes.
TD6			Threshold DAC input data bit.
QUAL ENABLE	A3J1 ($\overline{19}$)	A1J1	Control line for S.A. function mode. High during QUAL S.A., Totalize, and frequency. Low during NORM S.A.
TD7			Threshold DAC input data bit.
UNSTABLE	A3J2 (28)	A4	Drive line for front panel UNSTABLE annunciator LED.
UNCAL	A3J2 (29)	A4	Drive line for front panel UNCAL annunciator LED.
X1-X4	A3J2 (10, 24, 5, 20)	A4	Row enable lines from A1 Keyboard Encoder to A4 Keyboard matrix.
Y1-Y5	A3J2 (9, 25, 23, 21, 19)	A4	Column enable lines from A1 Keyboard Encoder to A4 Keyboard matrix.
10 MHZ	A3J1 ($\overline{16}$)	A1J1, A2J1	10 Megahertz reference signal from A3 oscillator. Distributed through instrument, and used to generate 5 MHz X1 and X2 microprocessor clocks.

8-88. 5005A THEORY OF OPERATION

8-89. Introduction

8-90. The following paragraphs provide the theory of operation for the 5005A Signature Multimeter. Included is a general instrument description, block diagram description, and a detailed circuit theory.

8-91. General Instrument Description

8-92. The 5005A Signature Multimeter is a multipurpose instrument featuring Signature Analysis as well as frequency, time interval, totalizing, dc voltage, Δ volts, peak volts, and resistance measurement capability. Refer to the Simplified Block Diagram in *Figure 8-13.*

8-93. A microprocessor monitors and directs the overall instrument operation. The microprocessor accesses the onboard RAM and ROMs through the DATA/ADDRESS and CONTROL buses. Data and control instructions for the rest of the instrument are sent and received through the I/O ports of the RAM and ROM modules.

8-94. The measurement function is selected via the front panel keyboard. Pressing any key generally produces a microprocessor interrupt, which alerts the the microprocessor to check the status of the keyboard. The microprocessor then proceeds to configure the various assemblies for the desired measurement, as per instructions stored in ROM. Completed measurements are routed over the DATA/CONTROL lines to the Display.

8-95. Signals are input to the 5005A through the Data Probe and/or the Timing Pod. The Data Probe is used in all functions except the time interval measurement. The Timing Pod is used for Signature Analysis, totalizing, and time interval measurements.

8-96. The Input Signal Switching circuits route the input signals to the appropriate assemblies. The microprocessor controls the signal switching function. The data is passed over the DATA/CONTROL lines. Data can be stored in the RAM, manipulated by the microprocessor, and routed over the DATA/CONTROL lines for display.

8-97. Analog measurements for the volts and ohmmeter functions are performed by the Digital Voltmeter. Digital measurements, including frequency, time interval, totalizing, Peak Voltage, and Signature Analysis are performed by the Digital Measurement circuits.

8-98. The Simplified Block Diagram in *Figure 8-13* illustrates the relative division of the functional circuits by actual assembly.

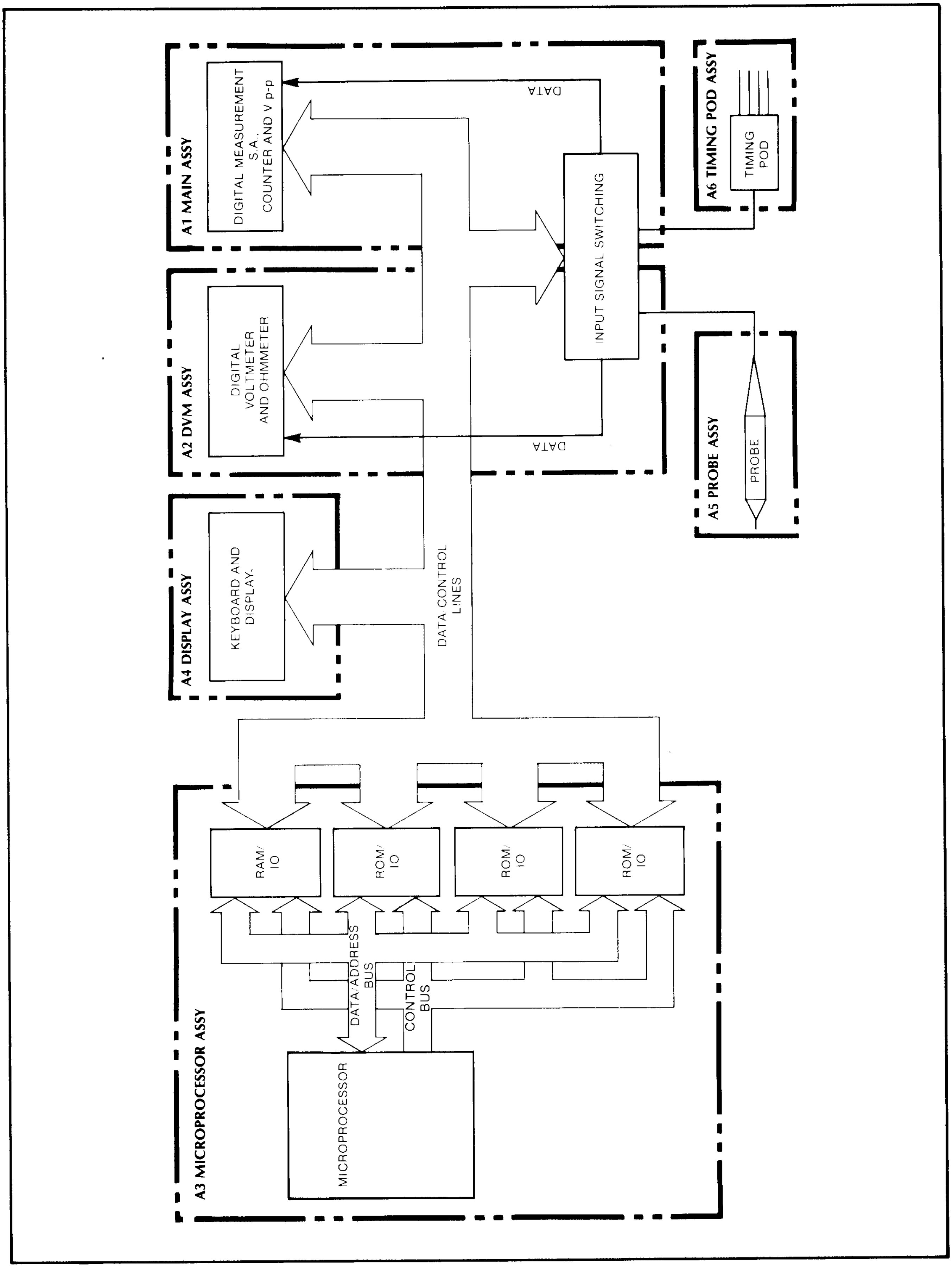

A1 MAIN ASSY
DIGITAL MEASUREMENT
S.A.,
COUNTER AND V p-p
DATA
INPUT SIGNAL SWITCHING
A6 TIMING POD ASSY
TIMING
POD
A2 DVM ASSY
DIGITAL
VOLTMETER
AND OHMMETER
DATA
A5 PROBE ASSY
PROBE
A4 DISPLAY ASSY
KEYBOARD AND
DISPLAY
DATA CONTROL
LINES
A3 MICROPROCESSOR ASSY
RAM/
IO
ROM/
IO
ROM/
IO
ROM/
IO
DATA/ADDRESS
BUS
CONTROL
BUS
MICROPROCESSOR

Figure 8-13. 5005A Simplified Block Diagram

8-99. BLOCK DIAGRAM DESCRIPTION

8-100. The following paragaraphs provide a block level description and refer to the Detailed Block Diagram in *Figure 8-20.*

8-101. MEASUREMENT TECHNIQUES

8-102. The 5005A makes measurements on both analog and digital signals. During any of the Volts or Ohms function modes, the instrument utilizes analog to digital measurement techniques. During Signature Analysis, Frequency, Time Interval and Totalize function modes, the 5005A operates in a digital mode.

8-103. The Power Supply on the A1 Main Assembly takes the input line voltage, transforms it down to plus and minus 20 volt ac sources, which are rectified, then input to four dc regulator circuits, which provide the + and -12.0, +5.0, and -5.2 dc volt supplies used throughout the instrument.

8-104. Depending on the selected function mode, input signals are received through the A5 Data Probe and/or the A6 Timing Pod assemblies. The Data Probe and Timing Pod input assemblies attenuate the input signals by a factor of 10, via Passive Divider networks. Signals from the Timing Pod are fed directly to the Input Voltage Comparators on the A1 Main assembly. Signals from the Data Probe are routed through the Data Switch Relay to the Input Voltage Comparators. The reference threshold voltages for the high-speed voltage comparators are generated by four Trigger Threshold DACs (Digital-to-Analog Converters). The DACs transform digital threshold information, determined by the front panel control settings and stored in RAM (ROM for default values), into the analog reference threshold voltages. The value of the threshold voltage determines the logic family and trigger levels of the signals at the inputs.

8-105. The outputs of the respective voltage comparators are level-shifted, via ECL-to-TTL Translators, and routed through Synchronizing and Edge-Select circuits. The Edge-Select circuits, directed by the status of front panel keys, determine which transitions of the Data Probe, START, STOP, and CLOCK signals are used for measurement timing, and the polarity level of the QUAL input signal. The output of the Data Probe comparator also drives the Data Probe Light Driver, which detects logic high, logic low, three-state, and active data states of the probe. These conditions are displayed by lighting, unlighting, dimly lighting, and flashing, respectively, the Logic State Indicator lamp within the Data Probe Tip.

8-106. After edge-selection, the signals are routed through the Data and Clock Selector Logic circuits, to the Feedback Shift Register/Counter (FSR) circuits. The microprocessor, responding to front panel operator selections, directs the Selector Logic to route specific signals to the circuits required to perform the desired measurement. The configuration of the Selector Logic along with the operating mode of the FSR determines the measurement function. The microprocessor controls the Selector Logic, and configures the Feedback Shift Register. The FSR can be configured as a shift-register or a standard accumulating counter, depending on the measurement. The possible configurations and operating modes of the FSR are as follows:

a. During both Signature Analysis modes (NORM and QUAL), the FSR is configured as a shift-register with feedback. This configuration, referred to as a puesdo-random-bit-sequencer counter (PRBS), allows the FSR to perform the S. A. measurement algorithm.

b. After all measurements, the FSR is automatically re-configured as a serial shift-register, which is used by the microprocessor to read out accumulated or residue measurement data. The data is serially output to the microprocessor system, where it is processed, formatted, and routed to the Display Decoder Driver. The Display Decoder Driver receives, decodes, and then displays the result.

c. During frequency and time interval measurements, the FSR is configured as a accumulating counter. For frequency measurements, the Selector Logic routes the Data Probe input into the counters, and gates the data in for the 5005A's preset one second gate period. For time interval measurements, the internal 10MHz clock, produced by the 10MHz Clock Generator on A3, is routed into the counters, and is accumulated for the duration between the Start and Stop inputs on the Timing Pod.

8-107. For analog inputs during voltage measurements, dc voltage applied to the A5 Data Probe is routed through Input Relays on A1, through the DVM Relays on A2, to the Attenuator, which if necessary, can divide the voltage by a factor of 10 or 100. After attenuation, the voltage is routed to the Analog section of the Analog-to-Digital Converter where it is converted to digital data, using the sucessive approximation method. The Digital section then generates the appropriate Digit, Sign, and a 4-bit BCD code information which is sent, via the I/O, to the microprocessor. The microprocessor decodes, processes, and sends it to the Display Decoder Driver circuits, which in turn route it to the A4 Display Assembly where the data is displayed.

8-108. The Analog Crosspoint Switches on A2 form a 4×4 switch matrix, which is used to route analog calibration voltages, and activate the appropriate attenuation circuit. The microprocessor determines the selections, and controls the switch.

8-109. Resistance measurements are performed by comparing the voltage across a known calibration resistor with the voltage across the unknown resistance (between the Data Probe Tip and ground). The known calibration resistor (Reference Resistance) is located within the Data Probe. The 2.0 Volt Reference Generator on A2 is used with the Reference Resistance to generate the reference voltage. The DVM measures the voltage, and the unknown resistance is computed by the microprocessor. Overvoltage protection is provided, via relays, in case the Data Probe is mistakenly placed across a voltage source while in a resistance function. When OVOL, from the A2 Overvoltage Detector, goes high, Reset 5.5 on the Microprocessor is pulled, which causes the A2 K1 and K2 relays to be activated, isolating the Data Probe and DVM from the source.

8-110. FUNCTION MODE DESCRIPTIONS

8-111. The microprocessor responds to Keyboard interrupts by reviewing the status of all front panel keys. The microprocessor directs the Keyboard Encoder circuits on A3 to scan the keyboard matrix on A4, and stores the results in RAM. This allows the microprocessor, by using the Selector Logic, Relays, and Analog Crosspoint Switches, to configure the instrument circuitry for any selected function mode and parameters. The following paragraphs describe the basic measurement configuration for each of the major function modes, and refer to the Detailed Block Diagram in *Figure 8-20.*

8-112. In general, pressing any front panel key will cause a microprocessor interrupt condition to occur. The microprocessor will respond by identifying the activated key and configuring the instrument accordingly. The catagories of possible key selections during most function modes are as follows:

*Mode change

*Edge or Level Select change

*Logic Family and/or Threshold Adjustment change

a. A Mode change occurs when the user presses a FUNCTION key other than the current operating mode. The microprocessor automatically senses the key selection and reconfigures the instrument to the selected mode.

b. An Edge Select change or Level Select change occurs when one of the front panel POLARITY keys is pressed. This causes the microprocessor to re-program the Edge Select and Level Select circuitry on the A1 Main Assembly, to respond only to the set conditions. Note that only the edges or levels used in the currently active function mode (as indicated by lighted front panel LEDs) are affected.

c. Threshold reading request or level change occurs when one of the currently active THRESHOLD keys are depressed. Note that only the thresholds currently being used have their LED indicators lighted. When a threshold reading request is activated (by a keypress within the THRESHOLD section) the microprocessor recalls the currently active threshold setting and displays it on the front panel, with the appropriate H (for High logic state) or L (for Low logic state) designations. The operator can change the active threshold level by changing logic families or by pressing the slew keys (with arrows) when the thresholds are being displayed. Internally the microprocessor interprets the keypresses and programs the DACs on the A1 Mainboard to the new active levels.

An intermediate or "null" logic level, used during Signature Analysis by the Data Probe, is produced by the Pull-to-Voltage Generator. The active logic levels selected for the Data Probe by the Trigger Threshold DACs drive the analog divider circuits within the Pull-to-Voltage Generator. The output is a buffered level at the midpoint (or logic null) between the high and low logic levels.

8-113. Signature Analysis Mode

8-114. Two modes of Signature Analysis operation are provided; NORM and QUAL. In the NORM mode of operation, the START signal comes from the START/ST-SP input and the STOP signal comes from the STOP/QUAL input of the 5005A Timing Pod. In the QUAL mode, both the START and STOP signals come from the START/ST-SP input and the QUAL signal comes from the STOP/QUAL input of the Timing Pod. This allows the framing of data within an operator specified Signature window.

8-115. SIGNATURE ANALYSIS/NORM MODE. During the NORM Signature Analysis mode, the input relays are programmed to route data from the Data Probe, and timing signals from the Timing Pod, to the Data and Clock Selector logic. The timing signals pass through Synchronizing and Edge Select circuits to the Data and Clock Selector circuits. After conditioning by these circuits the data is routed to the Feedback Shift Register where the Signature Analysis algorithm is performed. This data is read at the end of the measurement by the microprocessor through a serial data link from the A1 Main Assembly.

8-116. SIGNATURE ANALYSIS/QUAL MODE. The operation of the QUAL Signature Analysis mode is similar to the NORM mode, except that the START and STOP inputs are input on one line, and the measurement is "windowed" (gated) by the status of the QUAL input. The data is still input through the A5 Data Probe, and the aglorithm performed by the Feedback Shift Register remains the same.

8-117. kHz Mode

8-118. In the kHz Mode, the edge-select and threshold-select routines are performed as previously described for the desired levels. The Data Probe is the only active input in this mode. The microprocessor programs the input relays to route data to the Feedback Shift Register which is reconfigured by the microprocessor to be a totalizing counter. The microprocessor counts the number of overflows that occur, and the residue in the counter at the end of the measurement. It computes the total number of events during the fixed one second gate and displays this number as the frequency of the input. The gate light is flashed at a 1 Hz rate to indicate this gating function.

8-119. TOTLZ Mode

8-120. The TOTLZ Mode is similar to the kHz mode except the START and STOP inputs on the Timing Pod are used to select the gate time instead of utilizing the fixed 1 second gate. The counter's contents are read at the end of the measurement, and the number contained is formatted and displayed.

8-121. ms Mode

8-122. The ms (Time Interval) mode uses the START and STOP signals from the Timing Pod to gate the 10MHz time base into the counter section. The time base pulses are totalized for a duration determined by the Start and Stop pulses. The microprocessor is interrupted when an overflow occurs. The total number of overflows that occur between the Start and Stop pulses are accumulated in one of the microprocessor's internal registers. The residual time base pulses are contained in the Feedback Shift Register. This number is read at the end of the measurement by the microprocessor and a time interval is computed and displayed.

8-123. DCV Mode

8-124. In the DCV (DC volts) mode, the microprocessor configures the A1 input relays so the voltage at the Data Probe tip appears at the Data/Cal Relay of the A2 DVM assembly. The Data/Cal relay routes the signal past two switchable attenuators, to the A/D Converter, within the DVM. The attenuators are controlled by the Analog Crosspoint Switch under the direction of the microprocessor. The signal is either attenuated by X10 or X100. The selected attenuation factor is determined by the autoranging algorithm, stored in ROM. The Analog Section of the A/D Converter, in conjunction with the Digital Section, computes the voltage of the input. The DVM uses the precision 10.00 volt reference for an input for the measurement and the 10 MHz timebase signal (divided by 61) for timing purposes. At the end of the measurement the computed Voltage is acquired by the microprocessor which formats and displays the results of the measurement.

8-125. The incoming signal is checked by the Overvoltage Detector for excessive voltage. If the voltage extremes at the probe tip are more positive than +2.95 volts or more negative than +0.9 volts respectively, the microprocessor is flagged. The microprocessor immediately responds by isolating the probe from the 5005A, via a relay. The Overvoltage mnemonic (OL/OLOL) is displayed, while the instrument waits a fixed time interval before attempting the measurement again.

8-126. Delta V Mode

8-127. The Delta Volts Mode is similar to the DCV mode, except that the microprocessor accepts the first voltage measurement (performed when the Delta V key is pressed) as the reference. This voltage value is stored, then subtracted from the result of each successive measurement. The difference value is then displayed.

8-128. K ohms Mode

8-129. The k Ohms mode utilizes the voltmeter to produce a resistance measurement. The Precision 10.00 volt source is divided to obtain a Precision 2.00 volt source. The 2.00 volt source drives a 20 k ohm resistor placed in series with the unknown resistance to ground. This is achieved via the Data Probe with the programmed relays. The DVM circuits compute the voltage at the node between 20 k ohm resistor and the unknown. The microprocessor acquires the voltage and proportionally computes the unknown resistance.

8-130. VP+ and VP- Mode

8-131. For the VP+ and VP- modes, the input signal is routed via the input relays to the Input Voltage Comparators. The Trigger Threshold DACs are programmed by the microprocessor to find the peaks of the incoming signal. This is achieved with a successive approximation method of outputting incremental voltages by the DACs until the comparators change state or trigger. This trigger point is displayed by the microprocessor. Note that the microprocessor knows the trigger point because it keeps a record of the programmed DAC voltage.

8-132. DETAILED CIRCUIT THEORY

8-133. The following paragraphs provide the detailed circuit theory for each assembly within the 5005A. The theories are presented in numeric order, by assembly number, and reference the individual assembly schematic diagrams in *Figures 8-21* through *8-25*.

8-134. A1 MAIN ASSEMBLY

8-135. The A1 Main Assembly contains the Power Supply and Cooling Fan, Input Circuitry, Trigger Threshold DACs, Edge-Select and Synchronization circuits, Data and Clock Selector Logic, and the Feedback Shift Register.

8-136. Power Supply

8-137. The 5005A power supply provides six dc voltages; an unregulated + and -20 volts, as well as regulated, +5, -5.2, +12, and -12 volts. Power transformer T1 converts the line voltage input from the A7 Line Module, into two 14 Vac secondary voltages. Each secondary is rectified with a fullwave bridge network, CR5 and CR6, providing an unregulated -20Vdc and +20Vdc, respectively. The unregulated +20 volt line feeds +12 volt regulator VR3, and the +5 volt regulator circuitry U25, Q2, and CR6. VR3 is a simple three terminal regulator. U25 and it's support circuitry form a switching type regulator for the +5 volt power.

8-138. U25 monitors the +5 volt output, through the R62/R64 resistive divider, at pin 16. The dc level at pin 16, typically +4.9 volts, controls the variable duty cycle of the ~25 KHz pulse train output at U25, pins 8 and 11. The pulse train drives the base of switching transistor Q2, through R57. The duty cycle of the pulse train determines the amount of time Q2 is switched on and off, thereby regulating the amount of current supplied by the +5 volt supply. Should the supply be loaded down, the dc level at U25 pin 16 would drop, causing the duty cycle at pins 8 and 11 to change, remaining low for a longer percentage of time. Q2 would be switched on proportionally longer, supplying the additional current to the load. When the load is removed, the regulator returns to its quiesent operating condition. Diode CR8 is an over voltage protection diode limiting the output to six volts. Resistor R52 is used to eliminate start-up problems associated with pin 1 falling below ground. On start-up R52 keeps pin 1 and 15 of U25 (TL494) above ground. Inductor L2 is the primary energy storage device and diode CR7 provides a current path when Q2 is shutoff. The unregulated +12 volts drives the Fan Control and Fan B1. The unregulated -20 volts feeds the three terminal -12 volt regulator VR1, which in turn feeds the -5.2 volt regulator VR2.

8-139. Input Circuity

8-140. The A1 Main Assembly receives the four main input signals, DATA, START/ST-SP, STOP/QUAL, and CLOCK, from the A5 Data Probe and A6 Timing Pod. The three signals from the Timing Pod, START/ST-SP, STOP/QUAL, and CLOCK, are directly fed to the positive inputs of Input Voltage Comparators U6C, U6D, and U6E, respectively. The Data Probe signal is routed through the Data Switch Relay K2, to the positive inputs of U6A and U6B. The alternate output of the dual N.O./N.C. relay, routes the Data Probe signal to the A2 DVM Assembly during volt and ohmmeter functions. The Pull-to-Voltage Relay, K1, is used to route reference voltage to the 20 k ohm reference resistor within the A5 Data Probe during the ohmmeter function. The input relays are controlled via the microprocessor by control lines $\overline{K3}$ and $\overline{K4}$.

8-141. Variable capacitors C7 through C10, along with their resistive networks, provide adjustable input compensation for the four input signals. These circuits allow the input response to be tuned for minimum overshoot and undershoot. The negative (or reference) inputs for the Input Voltage Comparators come from the Trigger Thresholds DACs, described in following paragraphs. The outputs of the Input Voltage Comparators are routed through ECL/TTL logic translators U11 and U12, to their individual Edge-Select, U17A-D, and Synchronizer, U18 and U21, circuits. The signals are then input to the Selector Logic, which configures the signals for the desired measurement. The Selector Logic includes the Data and Clock Selector, U3, and the Start/Stop Selector, U16.

8-142. Trigger Threshold DACs

8-143. The four Trigger Threshold DACs, U1, U4, U7, and U13, transform digital information from the microprocessor into analog voltage, used by the input circuits to set the individual logic thresholds. The DAC inputs are connected in parallel. Eight bits of digital information are placed on lines TD0-TD7, by the microprocessor. Control lines DA0 and DA1 set up DAC Address Decoder U2, a one-of-four decoder, whose outputs drive the latch enables (pin 10) of each DAC. When the data strobe line $\overline{DSTR}$ goes low, the DAC threshold data is latched into the desired DAC. Each DAC has dual-polarity current outputs, which drive Op-amps, U14A through D, configured as current-to-voltage translators. The outputs of the Op-amps are routed through resistor voltage-dividers and filters, to the negative (or reference) inputs of the five high-speed Input Voltage Comparators, U6A-E. The circuit configuration allows for a single separate programmed threshold level for the Clock, via U13; the Start and Stop inputs, via U7; and two threshold levels (logic high and logic low) for the Data Probe input, via U1 and U4.

8-144. During DVM modes, the Data Switch Relay K2, is activated, routing the dc voltage level to the A2 DVM assembly through A1W2. The positive inputs to the Input Voltage Comparators are effectively pulled to ground through 10K resistors. The microprocessor, between voltage measurements, manipulates the DAC input data lines, performing a successive approximation routine, looking for the change of state level. Since the positive inputs are tied to ground, the voltage at which the comparators switch represents zero offset (the threshold level error due to leakage through the 10K resistors). The change of state from each comparator is routed through the ECL/TTL translators, U11 and U12, through threshold synchronizer U18 and Edge Selector U17C, to the Main Data Path. The DATA (PROBE) signal taps off Main Data Path, and is output on J1 pin 28 to the A3 Assembly, where it signals the microprocessor the zero offset has been found. The offset values, determined for each comparator, are stored on the A3 Microprocessor Assembly, and recalled and inserted as correction factors during the generation of input threshold levels.

8-145. Feedback Shift Register and Control Logic

8-146. The Feedback Shift Register (FSR) is comprised of four synchronous binary counters, U8, U9, U15 and U19, basically configured as a shift register (i.e. A output to B input). Exclusive OR/NOR gates, U5C and D, allow feedback of selected bits from each stage of the FSR to the inputs of the first two counters, U8 (pin 3) and U9 (pin 3), forming a puesdo-random-bitsequencer counter. During standard count modes, the FSR is set up as a divide by two (to the 16th) counter. F/F U20B acts as a divide by two prescaler to the FSR, producing a divide by two (to the 17th) counter, whose least significant bit is output by U20B (pin 9).

8-147. The FSR is used to accumulate and modify data in digital measurement modes. The actual operation of the FSR varies slightly, dependent upon the selected function mode. The following paragraphs describe the useage of the FSR during the three primary measurement configurations; Signature Analysis, Frequency and Time, and Data Read functions.

8-148. Signature Analysis Function

8-149. Three timing signals are required to make Signature Analysis (SA) measurements on data streams through the Data Probe; Clock, Start, and Stop.

8-150. The Clock signal, input through the Timing Pod, enters the A1 Main Assembly, through R2, to the positive input of Voltage Comparator U6E (pin 19). The negative input (pin 14) of U6E is the threshold reference input. This threshold reference voltage is provided by the Clock DAC U13, under control of the microprocessor, and represents the front panel threshold level selection. The detected clock, from U6 (pin 17), goes to the inverting input of the ECL/TTL translator U11B. The level-shifted clock signal then goes to the clock Edge-Selector U17D (pin 12). U17D is an exclusive-OR, which passes either a normal or inverted version of the input signal, determined by the CLOCK EDGE signal on U17 (pin 25). When the CLOCK EDGE line is high, U17D acts as an inverter. When it is low, the clock signal is passed unchanged. The output of the Edge-Selector U17D (pin 11) is routed to the Clock Selector, U3 (pin 11). The Clock Selector is controlled by the microprocessor through control lines COUNT and SIGNATURE-TI. When COUNT is low and SIGNATURE-TI is high (binary 01), U3's number "one" input lines (pins 5 and 11) are selected. The Clock Selector, U3, output (pin 9) drives the clock inputs (pins 2) of the FSR counters U8, U9, U15, and U19.

8-151. Start and Stop signals are required to define the measurement window. In the NORM Signature Analysis mode, the Start signal is input through the A6 Timing Pod to the Voltage Comparator U6C (pin 5). The Voltage Comparator output (pin 10) goes through ECL/TTL translator U11C, to Edge-Selector U17B, which either inverts the signal or passes it directly, depending on the level of START EDGE, at U17B (pin 5). When START EDGE is high, U17B acts as an inverter. When START EDGE is low, the signal is passed unchanged. After edge-selection, the signal is inverted by U5B, and input to the Start/Stop Synchronizer U21A. The true and complemented signals at pins 6 and 7 of U5B are utilized as asynchronous start and stop signals during T.I. and Totalize functions. The true and complemented signals at pins 5 and 6 of U21A are synchronous to the Main Clock and are utilized during Frequency, Period, and NORM Signature Analysis modes. The four Start/Stop signals are input to the to the Start/Stop Selector, U16 (pins 12,13,14,15). The output of the Start/Stop Selector U16, clocks control flip-flops U10A, U10B, and U20A. U10B output pin 9 goes high, which removes the Reset condition from all four FSR counters (U8, U9, U15, and U19), which enables them to start the measurement. The complemented output of U10B (pin 7) is inverted through U2B, and output as GATE on J1 pin 27. This signal is routed through the A3 assembly, to the A5 Display where it drives the front panel Gate LED.

8-152. The Stop signal is input through the A6 Timing Pod, to the Input Voltage Compararator U6D (pin 8). The Voltage Comparator output (pin 11) goes through ECL/TTL translator U11D, to the Edge-Selector U17A. The STOP/QUAL EDGE line determines whether the Stop signal is inverted or passed unchanged. After edge-selection, the signal is routed to the Start/Stop Selector, U16 (pins 3,4), and to exclusive-OR/NOR U5A. Pin 1 of U5 is tied to ground, so the Stop signal is passed unchanged to the data input (pin 12) of the Start/Stop Synchronizer, U21B (pin 12). U21 synchronizes the Stop signal to the Clock. The synchronized Stop signal passes from U21B (pin 9) to the Start/Stop Selector U16 (pins 1,2). The selected Stop output from U16 clocks control flip-flops U10A,B and U20A, sending U10A (pin 5) high, which produces END OF MEASURE (J1 pin 30). This flags the microprocessor, signaling the measurement is complete. When U10 pin 5 goes high, pin 6 goes low, which disables the FSR counters (U8, U9, U15, and U19) through OR-gate U26D.

8-153. In the QUAL mode, the Stop signal is input through the A6 Timing Pod, on the same line as Start (START/ST-SP). Both the Start and Stop signals are processed through the same input circuits up to the Start/Stop Synchronizer. U21A becomes the synchronizer for both the Start and Stop signals. The outputs from U21A (pins 5 and 6) are the true and complemented Start signals. These signals are input to the Start/Stop Selector on pins 12 and 13. The control line POLARITY DIFF works in conjunction with START EDGE to select either the positive or negative Start Edge as the desired Stop Edge during QUAL S.A. POLARITY DIFF comes in through U26C, to pin 11 of the Start/Stop Selector U16. Pin 11 is the LSB of the binary select lines, determining whether an odd or even input is selected; whether pin 13, the true Start Edge, or pin 12, the complemented Start Edge, is selected. $\overline{\text{COMBINED START/STOP}}$ goes low, enabling U26B, which allows selection of the four higher order inputs (4 through 7) by the Start/Stop Selector.

8-154. The QUAL input comes in through U6D and U11D, to Edge-Selector U17A. The output at pin 6 goes through Exclusive OR/NOR U5A, and passes unchanged to the data input of the Start/Stop Synchronizer U21B. QUAL ENABLE goes high in the QUAL mode, enabling gate U26A to pass the QUAL signal through as enable (low) or disable (high) for the FSR counters.

8-155. Frequency and Time Interval Functions

8-156. The Frequency, Time Interval, and Totalize functions are similar, in that the FSR is configured as a accumulating counter counting asynchronous events input through the A5 Data Probe. The differences are in the methods of gating the FSR. For Frequency the FSR is gated through timer circuitry on the A3 Assembly, which generates one second gate periods between readouts. The Time Interval and Totalize modes use external Start and Stop signals, through the A6 Timing Pod, to window the measurement.

8-157. During a frequency measurement, the signal is input through the A5 Data Probe, through the Data Switch Relay K2, to the Input Voltage Comparators. Two voltage comparators, U6A and U6B, are required for the Data Probe input signal. This allows DAC threshold control over both the high (H) and low (L) logic level for all logic families. The outputs of U6A and U6B represent the duty cycles of the active low and high trigger thresholds. These outputs are level-shifted through ECL/TTL translator U12B and U12C, inverting U6A, and input to the "J" and "K" inputs of the Probe Synchronizer U18A and U18B. The output of U6A is also routed through ECL/TTL translator U11A, whose output helps drive the Data Probe Light Driver U24. U18 is not used for synchronization in this mode, but rather configured as an RS F/F, setting and resetting on the edges of the high and (inverted) low data probe signals, through U22A. U22A is a 2-to-1 data selector, controlled by the SYNC line from the microprocessor, used to determine the Set and Reset for U18A and U18B. U18B is not used in the frequency mode.

8-158. The resulting output from U18A (pin 5) is a waveform representing the duty cycle of the active triggering period. The output from pin 6 is the true facsimile of the input signal. This output is routed directly to pin 4 of the Data Selector U3. The Data Selector directs input "1" during S.A., input "2" during Frequency, and input "3" during T.I. The selected output is routed through U5C, as input to the Feedback Shift Register.

8-159. During a time interval measurement, the Start and Stop signals enter the Timing Pod, and are processed just as for the NORM S.A. measurement mode. These signals define the measurement counting window. Microprocessor control lines SIGNATURE-TI and COUNT will be high, causing Data Selector U3 to route the internal 10 MHz Oscillator signal to the FSR counters. The FSR, configured as a counter, will accumulate 10 MHz clock pulses for the duration set by Start and Stop. After the Stop is received, END OF MEASURE is generated, signaling the microprocessor to perform a Data Read on the counters.

8-160. Data Read Function

8-161. After any measurement, sixteen bits of data are serially read out of the FSR on U19 pin 11, and output as REGISTER DATA on J1(28), into the microprocessor system at A3 U4 pin 34. When in count modes, the seventeenth bit is developed by flip-flop U20B and output as LSB COUNT on J1(29).

8-162. Coincident with the Stop signal is the END OF MEASURE signal from U10A (pin 5). A high on this flag signals the microprocessor that the measurement is complete. The microprocessor sends QUAL ENABLE low, forcing U26A high and U26D low, enabling the shift mode on FSR counters U8, U9, U15 and U19. The microprocessor reads the LSB COUNT line, from U20B (pin 9), and $\overline{\text{OUTPUT SHIFT ENABLE}}$ goes low, which resets U10A, clearing END OF MEASURE (pin 5). DATA STROBE, from the microprocessor, is then routed by Clock Selector U3, to clock the data out of U8, U9, U15, and U19 through U19 (pin 11). Each DATA STROBE pulse moves one bit out of the FSR.

8-163. During count modes, the FSR is configured as a divide by two (to the sixteenth), with an additional bit of resolution (divide by two to the seventeenth) provided through divide by two prescaler U20B. Normal inputs can overflow the counting ability of the configuration. The microprocessor provides an interrupt every 250 microseconds. During that interrupt, the REGISTER DATA bit (MSD) is examined. Whenever a transition is detected, indicating the counter is full, the microprocessor assumes an overflow has occured, and stores the overload bit within an internal register. The count in the counter rolls over to all zeros with the next clock. At the end of the measurement, the number of overflows is combined with the residue count in the FSR to calculate the total number of events.

8-164. The GATE output pin $\overline{27}$ basically monitors the Measure Flip-Flop U10B, and determines when the FSR is accepting data, when a measurement is in progress. The GATE signal is routed through A3, to the A4 Display Assembly, where it drives the Gate Light LED.

8-165. A2 DVM ASSEMBLY

8-166. The A2 DVM Assembly contains the circuitry necessary for the voltage and resistance measurement functions of the 5005A. The A2 DVM Assembly contains the input DVM relays, Attenuators, Clock Divider, A/D Converter, Analog Crosspoint Switch, and various protection and voltage reference circuits.

8-167. A/D Converter

8-168. The basic function of a voltmeter is to convert an analog input voltage level to digital data, which can then be processed and displayed by the microprocessor system. This function is performed by two LSI chips, U4 and U7, which form a 4 1/2 digit A/D Converter. U4 is the Analog Section and U7 is the Digital Section.

8-169. The A/D Converter desired measurement input voltage range is from -2.5 to +2.5 volts, at its input (pin 15). Two attenuators allow the input voltage to be scaled by a factor of 10 or 100. This configuration allows three ranges of input voltage; ± 2.5 volts, ± 25 volts, and ± 250 volts, depending on which, if any, attenuators are active. At no time does the actual voltage to the A/D Converter circuits exceed ±5.0 volts, due to the voltage clamps formed by Q1 and Q2.

8-170. During a voltmeter function, one of the attenuators is always on, selecting either the ± 25 volt (X10) or ± 250 volt (X100) range. The 2.5 volt range (no attenuation) is only used during the ohmmeter function. If the DVM's first measurement is greater than ± 2.5 volts, the microprocessor will direct the Analog Crosspoint Switch to turn off the X10 attenuator and turn on the X100 attenator. This automatically autoranges the voltmeter from a ± 25 volt range to the ± 250 volt range.

8-171. The attenuated input voltage appears at U4 (pin 15). The +8 volt reference at U4, pin 10 (REF IN), is formed by the resistive voltage divider of R9, R10, and R8. The buffered REF OUT, U4 pin 8, goes through R17 (100K) to the integrator input at U4 pin 9.

8-172. The digital section of the A/D Converter is U7. With its input from U4, U7 outputs data on four BCD lines, digit available on five lines, and Sign information. The BCD outputs are at U7 pins 9, 10, 11, and 12 with the LSB (B0) at pin 9. The Digit Available, D0 through D5, are output at pins 2, 1, 18, 17, and 16 respectively. The Sign output is at pin 13 and when high, indicates a positive voltage reading. The Start input to U7 is at pin 7 and comes from the microprocessor. The final input to U7 is the clock. The clock is approximately 164 KHz, generated by U8 and U9. U8 and U9 are connected to form a divide-by-61 circuit. The input to this circuit is pin 2, the internal 10 MHz clock. The 164 KHz output is U9 pin 13 which goes through level shifter Q6 to the "fOSC" input of U7, pin 8.

8-173. Voltmeter Function

8-174. During the Voltmeter function, input dc voltage enters through the A5 Data Probe tip, and is routed to the A2 DVM assembly by the Data Switch Relay on A1. The voltage enters A2 at J2, transfers through the DVM DATA/CAL Relay K2, through series resistor R5, to the V-in input of U4 (pin 15). FETs Q1 and Q2 clamp the input line to +5 volts and -5 volts, respectively, to prevent a dc level greater than 5 volts from reaching the input of U4. The FET circuits Q4/R6 and Q3/R7 form the X10 and X100 Attenuators. *Table 8-3* shows the Attenuator control for each of the three ranges. The attenuators are activated via the Analog Crosspoint Switch, which decodes binary information from the microprocessor system, directing either +10.00 volts or GND to the gate of the desired FET. Switching GND to a FET will turn it on (saturation), switching +10.00 volts will turn it off.

8-175. In the 25 volt range, Q4 is turned on placing R6 in the circuit. The combination of A5R1 (89.6k), A2R5 (10M) and R6 (1.1M) form a 10.1 voltage divider which attenuates the input by 10. In the 250 volt range, Q4 is turned off and Q3 is turned on, placing R7 in the circuit. The combination of A5R1 (89.6k), R5 (10M) and R7 (100K) form a 100.1 voltage divider which attenuates the input by 100. In the 2.5 volt range, both attenuator FETs are turned off.

Table 8-3. DVM Range Setting

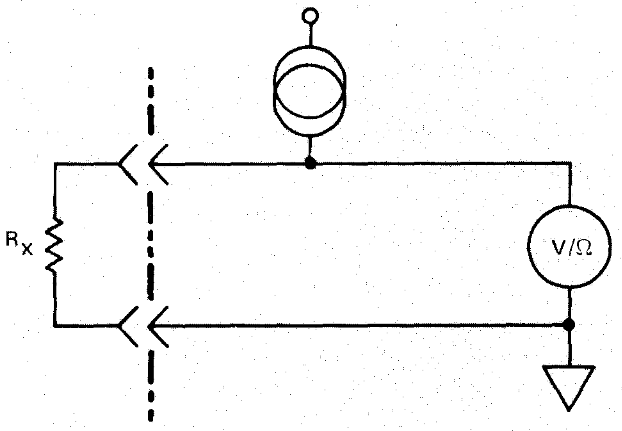
INPUT VOLTAGE RANGE	ATTENUATOR	Q4	Q3	U2 SWITCH ACTIVATED	
2.5000V (OHMS)	(X1)	OFF	OFF	S1	S2
25.000V	X10	ON	OFF	S13	S2
250.00V	X100	OFF	ON	S1	S14

8-176. Analog Crosspoint Switch

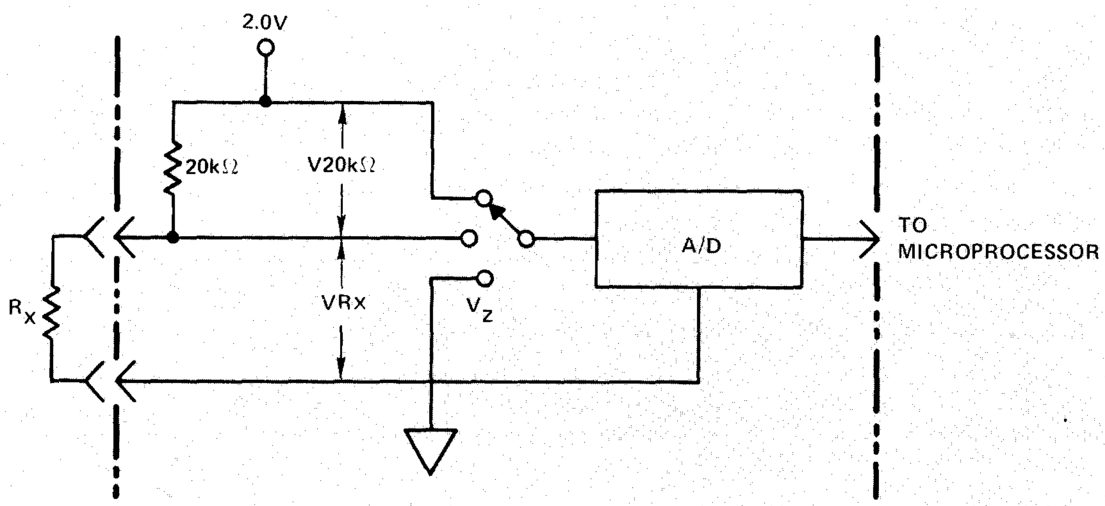
8-177. The enabling of attenuators Q3 and Q4 and the switching of calibrate voltages is performed by U2, which is a 4X4 Analog Crosspoint Switch. The microprocessor controls U2, through level shifter U5, by setting the switch address on lines A, B, C, and D (U2 pins 6, 5, 3, and 4); setting the desired switch status on SW, U2 pin 2 (1 for ON or 0 for OFF); and strobing this data through SW, pin 7. For example, when the voltage range is switched to the 25.00 V range, Q4 is turned on causing the input voltage to be divided by ten. The microprocessor then addresses U2 (switch 13) by placing 1101 on pins 4, 3, 5, and 6 respectively. Next, the microprocessor sends a clock to the SW input U2 pin 7. This causes switch 13 to close, allowing GND to be applied to the gate of Q4 which turns on, placing R6 (1.1M) into the circuit which causes the input voltage to be divided by ten.

8-178. Ohmmeter Function

8-179. In most ohmmeters, a constant-current source is output to the unknown resistor (Rx) and the voltage developed across Rx is then measured and displayed in ohms, as illustrated in the diagram below.



8-180. The disadvantages of this method are; (1) The current source must be precision and (2) there is limited range. The 5005A uses an alternate method which overcomes these disadvantages. The diagram below is the simplified circuit used by the 5005A.



8-181. The 5005A uses a 2.0V source and a resistor of known value. When measuring ohms, the voltage across the known 20.00K resistor is measured and the value is stored. Then, the voltage across the unknown resistor, Rx, is measured and stored. The microprocessor then determines the ratio of the two voltages and computes and displays the resistance value using the following formula:

$$Rx = \left(\frac{Vx - Vz}{2.0V - Vx} \right) 20K \text{ ohms}$$

Where:
Rx = Unknown Resistance
Vx = Voltage measured across Rx
Vz = Zero voltage (Ground)
2.0V = 2.0V reference

8-182. The circuits involved include U3, K1, and K2 on the DVM Assembly and R2 on the Data Probe. U3 acts as a buffer for the 2.0V source. The output of U3 (pin 6) goes through Ohm Control Relay K1 to Rx via the 20.00K resistor, R2, within the A5 Data Probe. Data/Cal Relay K2 allows the voltage to be read either across the unknown resistor, or the A5 Data Probe resistor in series with the unknown resistor. The voltages in the ohmmeter function are measured with both Q3 and Q4 off, selecting the 2.5V input range.

8-183. Resistance measurements are normally performed on passive components; i.e., components which have no voltage across them. If, however, the A5 Data Probe is placed across a voltage source while the 5005A is in ohms function, the Overvoltage Detection Circuitry, made up of U6 and Q5, automatically prevents the unit from being damaged. U6 is the overvoltage detector. The sense line connects the input of U6 (pins 3 and 6) through R24 (10K) to the 2.0V source. U6B triggers at the upper threshold (2.95V) and U6A triggers at the lower threshold (0.9V). The outputs (U6 pins 7 and 1) are wired-ORed, translated by Q5, and sent as an interrupt flag to the microprocessor, indicating overvoltage (OVOL). When an OVOL interrupt is received, the microprocessor responds by opening the Ohm Control Relay K1, and Data/Cal Relay K2, isolating the A5 Data Probe and the A2 DVM assembly from the source.

8-184. A3 MICROPROCESSOR AND DISPLAY DRIVE ASSEMBLY

8-185. The A3 Microprocessor Assembly monitors and directs the overall operation of the 5005A. The main functional blocks include the microprocessor, Power-Up Reset, 10 MHz Oscillator and Clock Generator, address and data buffers, ROM (Read Only Memory) with I/O, RAM Timer/Synchronizer and RAM (Random Access Memory) with I/O, Display Decoder Driver, and Keyboard Encoder.

8-186. All of the internal operations of the instrument are directed by the microprocessor system (or kernel). The kernel consists of the microprocessor, its associated address and data buffers and decoders, ROM (Read Only Memory) and RAM (Random Access Memory). The kernel operates by interpreting and responding to control programs, consisting of 6K bytes of 8085 assembly code, permanently stored in ROM.

8-187. The ROM and RAM devices are accessed by the microprocessor by placing an address on the Data/Address bus and either writing to or reading from the addressed device. The microprocessor CE, $\overline{RD}$ and $\overline{WR}$ output control lines determine which device is enabled. The ROM and RAM devices also contain I/O ports. These are used to control and direct the flow of data, back and forth over the buses. The I/O ports are contained within the RAM and ROM memory devices, but function totally independently. The microprocessor $\overline{IO/M}$ output control line selects between the I/O and Memory sections of the devices.

8-188. Power-Up Reset

8-189. When the LINE switch is turned on, +5 volts is applied to the Power-Up Reset circuit and the microprocessor. The +5 volts is integrated by the Power-Up Reset circuit, consisting of CR2, R29, and C16, generating a slow rising level at pin 36 of U16. The rise of the level is slow enough to provide a RESET interrupt (logic low) to the microprocessor. The delay generated is approximately 0.1 second, determined by the time constant set by R29 and C16. The level then remains high until the LINE switch is turned off.

8-190. CR2 provides a discharge path for C16 when power is removed. The RST IN reset to the microprocessor immediately directs it to fetch a "restart vector" from a fixed location in the ROM. This reset vector tells the microprocessor where to find the first routine that it is to execute, which is the Power-Up Self Check routine. This self-check routine runs tests on major circuits, and momentarily lights all the front panel LEDS for a operator's visual check. After a predetermined time, the program instructs the microprocessor to branch to the Norm Signature Analysis mode program.

8-191. Display Decoder Driver

8-192. The Display Decoder Driver U6, is a complete display interface, capable of receiving and storing eight eight-bit words of display data. U6 decodes the data, and drives the display devices (on A5), with it's self-contained multiplexed scan circuitry. The data is continously scanned into the display until the microprocessor signals a change in data, by pulling the MODE pin 9 low. Then, data is read directly from the microprocessor DATA bus, from lines A through H, automatically sequenced into U6's memory on successive negative going $\overline{\text{WRITE}}$ pulses.

8-193. Keyboard Encoder

8-194. The Keyboard Encoder U3, is a CMOS sixteen-key encoder, containing all the necessary logic to scan and encode the status of an array of SPST switches. Whenever a front panel key is pressed, DATA AVAILABLE (pin 13) goes high. The next clock pulse causes a high out on pin 5 of D-Flip-flop U5. This sends an interrupt (RST 6.5) to the microprocessor. The microprocessor responds by setting pin 3 of U9 low, activating the OUTPUT ENABLE for U3 and resetting interrupt flip-flop U5. The status of all the front panel switches is placed on the DATA bus through lines A through E. An internal register within U3 remembers the last key pressed. After the new switch status is stored by the microprocessor, the Keyboard Encoder returns to a monitor scan operation until another key is pressed. The DATA AVAILABLE line is also routed to the I/O of U4 pin 31, to notify the microprocessor the keypress is being held. This allows the microprocessor to discriminate between a normal keypress and the use of the ADJUST/NOISE MARGIN keys, which step up or down as long as the key is held. C6 sets the frequency of the internal scan oscillator, and C7 compensates for key bounce.

8-195. 10 MHz Oscillator and Clock Generator

8-196. The 10 MHz Oscillator U1, is the main timebase for the instrument. U1 is a hybrid three-terminal oscillator, which generates a 10 MHz squarewave at ≈ four volts p-p. The 10MHz output from pin 8 of U1 is buffered by Q1, and routed through R19 to J1 pin $\overline{16}$ to the other assemblies. R17 and Schottky diode CR1 insure Q1 remains biased on. R1, C1, C2, and C3 filter the +5 volt supply to U1. The 10MHz Oscillator output is also routed to the clock input (pin 11) of D-flip flop U5B. U5B is a divide-by-two Clock Generator, which produces the normal, and via inverter U10, complemented 5MHz clocks for the microprocessor X1 and X2 inputs.

8-197. Microprocessor

8-198. The A3 Microprocessor Assembly uses the Intel 8085 microprocessor U16. The microprocessor is the source of all major control of the 5005A. It is a fully contained processing unit that actively responds to the 5005A state and controls, and makes logic decisions. The microprocessor has eleven inputs, nineteen outputs, and eight multiplexed inputs/outputs.

8-199. Microprocessor Inputs

8-200. Seven of the eleven possible inputs are used. These are capable of halting the microprocessor. The inputs are described below.

8-201. X1 and X2. X1 and X2 are the clock inputs for the microprocessor. The true and complemented 5 MHz squarewaves from the divide by two Clock Generator are input to U16 on pins 1 and 2. These inputs provide all the timing and synchronization signals for the microprocessor system. An internal clock generator within U16 again divides X1 by two, producing a 2.5 MHz clock. This clock is also used within the microprocessor and output as CLK (pin 37), a control line to the microprocessor system.

8-202. $\overline{\text{RST IN}}$. The microprocessor $\overline{\text{RST IN}}$ input is generated by the Power-Up Reset circuitry. When power is applied to A3, an integrated dc level at U16 pin 36, rises from ground (logic low) to -5 volts (logic high), slowly enough to provide an active (low) reset interrupt to the microprocessor. This reset input directs the microprocessor to automatically fetch the restart vector from ROM, which properly references the microprocessor to the system program.

8-203. READY, RST 5.5, RST 6.5, and RST 7.5. These inputs are control signals used by the microprocessor. ROMs U4, U11, and U13 signal the microprocessor via the READY input. The reset inputs represent conditional interrupts; RST 5.5 indicates an overload or overvoltage state from the A2 DVM, RST 6.5 indicates a front panel key has been pressed, and RST 7.5 is a 250 microsecond interrupt, utilized during count modes to check for overflows.

8-204. Microprocessor Outputs

8-205. Fourteen of the nineteen outputs from the microprocessor are used. The outputs are described below.

8-206. ADRS LINES. The 8085 microprocessor has sixteen address lines, A0 through A15. The higher order lines, A8 through A13, are dedicated address control lines. A14 and A15 are not used. The lower order lines, A1 through A7, are combined with the Data bus lines, in a mutiplexed Address and Data Bus system. The Address lines of the microprocessor are used to logically address specific locations in the microprocessor address space. The functional blocks accessed by the address lines are the Keyboard Encoder U3, the ROMs U4, U11, U13, the RAM/Timer U8, and various control circuit blocks. All reside at a specific address or block of addresses as viewed by the microprocessor.

8-207. The following memory and I/O maps, *Tables 8-4* and *8-5*, list the addresses, and the addressed device, for the A3 Assembly. The H symbol in the address indicates a hexadecimal address.

Table 8-4. Memory Map

ADDRESS	ADDRESSED DEVICE
OH to 7FFH	ROM (U11)
800H to FFFH	ROM (U13)
1000H to 17FFH	ROM (U4)
3800H to 38FFH	RAM (U8)

Table 8-5. I/O Map

ADDRESS	ADDRESSED DEVICE
OH	ROM (U11) PORT A
1H	ROM (U11) PORT B
8H	ROM (U13) PORT A
9H	ROM (U13) PORT B
10H	ROM (U4) PORT A
11H	ROM (U4) PORT B
39H	RAM (U8) PORT A
3AH	RAM (U8) PORT B
3BH	RAM (U8) PORT C
8H input	Keyboard Controller
28H output	Display Controller
80H	Dummy I/O Port*

*Provides Start and Stop signals for another Signature Analyzer, for Diagnostic and Test purposes.

8-208. DATA LINES. The 8085 microprocessor utilizes a multiplexed Address and Data bus system. Lines AD0 through AD7 function as both lower order Address lines, and Data lines. The Address/Data bus functions as an Address bus during the first half of the microprocessor cycle and as a Data bus during the second half of the cycle. The microprocessor is designed to logically separate the signals transmitted on this bus and to place data on the bus for use by the microprocessor. Address and Data information is placed on the bus structure in eight or sixteen-bit parallel bytes.

8-209. CONTROL LINES. The remaining six microprocessor lines, ALE, RST OUT, CLK, IO/$\overline{\text{M}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$, are output Control lines. They are used for the control and timing of the microprocessor system. ALE, Address Latch Enable, notifies the RAM and ROM devices when bus address information is valid, instructing them when to latch the data in. RST OUT is a Reset, used to initialize or reset the I/O sections of RAM and ROM. CLK, Clock, is a 2.5 MHz squarewave, used as a master clock for sequence and of the RAM and ROM devices. IO/$\overline{\text{M}}$, I/O port/Memory, enables either the I/O port or Memory section of the RAM and ROM devices. The $\overline{\text{RD}}$, Read, and $\overline{\text{WR}}$, Write, lines are used to configure the RAM with I/O and ROM with I/O devices, to be read-from, or written-to, from the Address/Data bus.

8-210. Buffer Circuits

8-211. The bi-directional Buffer U14, is used to buffer and isolate the microprocessor Address/Data bus lines. U14 is also used to implement the freerun function for Signature Analysis. The direction of data flow is determined by the $\overline{\text{RD}}$ line from the microprocessor, via inverter U7.

8-212. Address Decoder U15 is used to decode address lines All, A12, and A13. This circuit generates the clock enables, $\overline{\text{CE}}$, $\overline{\text{CE1}}$, $\overline{\text{CE2}}$, and $\overline{\text{CE3}}$, for the RAM U8, and ROMs U11, U13, and U4. It also helps generate the $\overline{\text{OUTPUT ENABLE}}$ and $\overline{\text{WRITE}}$ for the Keyboard Encoder U3 and Display Decoder Driver U6.

8-213. ROM and I/O

8-214. The 5005A utilizes 5144 bytes of ROM, contained in three integrated circuits U4, U11, and U13. The circuits are capable of decoding the multiplexed AD0-AD7 bus, utilizing the other control lines from the microprocessor. When addressed, the ROMs place the data contained in the addressed location on the Address/Data bus, in eight-bit parallel bytes, for use by the microprocessor.

8-215. Two eight-bit I/O ports are also contained within each integrated circuit. When the I/O portion of the integrated circuit is addressed, the I/O port can be written-to or read-from depending on the previous programming. The I/O portion is programmed by writing to a specific location in the integrated circuit combined with certain conditions being met on the control lines. The IO/$\overline{\text{M}}$ line determines whether the I/O or the memory portion of the ROM is addressed.

8-216. RAM/Timer with I/O

217. U8 is the RAM/Timer with I/O. The RAM is addressed from memory location H3800 to H38FF. The Timer and I/O registers are addressed at defined I/O locations. The Timer is an essential element during frequency modes, used to generate the one-second gate. The 2.5 MHz CLK output from U16 pin 37, is routed to the TIMER IN pin 3 of ROM/Timer U8. This clock drives an internal programmable counter, which generates a microprocessor interrupt every 250 microseconds. The interrupt is output on TIMER OUT pin 6 which is routed as a RST 7.5 reset to the microprocessor. During frequency modes, an internal register within the microprocessor is preset to the number "4000". The register decrements with every RAM/Timer interrupt, while

the microprocessor checks for overflows in the FSR. At the completion of "4000" 250 microsecond periods, (the one second gate), the microprocessor turns off the GATE, and issues a series of control signals which turn off the Gate LED and change the configuration of the A1 Select Circuits.

8-218. Timer/Synchronizer

8-219. Timer/Synchronizer U12A is a D-flip-flop. U12A synchronizes the $\overline{\text{TIMER OUT}}$ signal from U8 pin 6, to the CLK output, pin 37, of microprocessor U16, to assure better accuracy.

8-220. A4 DISPLAY AND KEYBOARD ASSEMBLY

8-221. The A4 Display Assembly contains the six seven-segment LEDs used for the Display, the front panel keyboard, the Key Indicator LEDs, and some additional status display LEDS. The seven additional status display LEDS, consisting of DS15, DS16, DS19, DS23, DS24, DS25, DS29, are driven directly by lines from A3U2 and A3U4. All the remaining keys and LEDs are multiplexed, driven by buses from the A3 Microprocessor assembly.

8-222. Microprocessor A3U16 writes the characters and LED status information to the Display Decoder Driver A3U6. U6 properly sequences all strobes, segment lines, and LED drive lines, in a multiplexed configuration, before routing the display buses to the A4 Display Assembly. The main Data Display consists of five seven-segment LEDs, DS1 through DS5, and the polarity sign indicator DS6. Data for the Display is decoded on A3, and placed on the Display Data bus lines, "a through g, and dp", one digit at a time. As each digit's data is placed on the bus, the appropriate control line, DEVICE ENABLE 0 through 6, enables the corresponding seven-segment LED. The DEVICE ENABLE lines continuously cycle, strobing data into the Display LEDs. The Key LEDs and Status LEDs are configured into a matrix, selected and strobed by the same Display Data bus and DEVICE ENABLE bus lines as the main Display.

8-223. The A4 Keyboard, consisting of nineteen momentary-closure pushbutton switches, S1 through S19, is also configured into a matrix. The status of the switches is continuously monitored by nine lines, X1 through X4 and Y1 through Y5, from the A3 Keyboard Encoder. A3U3 detects when any key is pressed and generates an interrupt which is sent to the A3 microprocessor. The microprocessor responds by reading the Keyboard Encoder memory and resetting the Keyboard Encoder interrupt flip-flop A1U5.

8-224. A5 DATA PROBE ASSEMBLY

8-225. The A5 Data Probe contains the 10:1 Passive Divider, Reference Resistor, and Logic State Indicator lamp. Analog and digital data signals are input to the HP 5005A through the probe tip of the A5 Data Probe. The signals are attenuated by a factor of ten by the passive divider network consisting of R1, C1, in conjunction with A1R7 and A1R8. A5R2 is the 20k ohm Reference Resistor, used during the Ohmmeter function. DS1 is the probe Logic State Indicator, an incandescant lamp driven by the Data Probe Light Driver circuit on A1. There are no active components on A5.

8-226. A6 TIMING POD ASSEMBLY

8-227. A6 Timing Pod receives the three major timing signals for the HP 5005A; START/ST-SP, STOP/QUAL, and CLOCK. Each of the three signals passes through the first stage of it's own passive divider network. The remaining components for the final stage of each divider are located on A1. The signals are attenuated by a factor of ten as they are routed to the Input Voltage Comparators on A1. There are no active components on A6.

8-228. A7 LINE MODULE ASSEMBLY

8-229. The A7 Line Module Assembly is attached to the rear of the A1 Main Assembly. It contains the connector for the power cable, the line fuse, line input filtering, and a printed-circuit card. The printed-circuit card can be inserted in any one of four positions to select 100, 120, 200, or 240 volt ac operation. The schematic for the A7 Line Module Assembly is shown in *Figure 8-21*. A detailed description, including instructions for changing the fuse or voltage selection is given in paragraph 2-5.

8-230. TROUBLESHOOTING

8-231. Introduction

8-232. The HP 5005A is a microprocessor based system. The majority of the instrument circuitry consists of digital logic configurations. The primary method of fault location is through signature analysis, keyed to built-in Diagnostic routines.

8-233. The digital voltmeter, power supply, and much of the input circuitry including Data Probe, Timing Pod, comparators, and DACs are analog circuit configurations. These circuits are supported with more conventional troubleshooting techniques, including built-in Diagnostic routines as well as active signal tracing.

8-234. Troubleshooting information is provided through various troubleshooting procedures, described in this section. Diagnostic troubleshooting information is also provided in abbreviated form on corresponding assembly Service Sheets.

8-235. Troubleshooting Flowchart

8-236. The basic troubleshooting technique is illustrated in the Overall Troubleshooting Flowchart, *Figure 8-14*. No troubleshooting system or philosophy is failsafe. This flowchart attempts to show how best to interpret the indications provided by the Power-up Self Check, Error Messages, and Display to initially isolate the trouble. Individual troubleshooting procedures are provided for the Power Supply, Kernel, and Assemblies A1, A2, A3, and A4. The Overall Troubleshooting Flowchart should help direct the technician to the proper procedure. The use of the flowchart is described in Overall Troubleshooting, beginning with paragraph 8-245. Once familiar with the individual Diagnostic Procedures, the technician may proceed directly to indicated assembly Service Sheets for specific troubleshooting information and abbreviated Diagnostic Procedures.

8-237. Troubleshooting Aids

8-238. The 5005A provides a variety of built-in troubleshooting aids, within the firmware of the instrument. These include an initial Power-Up Self Check routine with corresponding Error Messages, and a series of user-designated Diagnostics. These aids are explained in detail in the following paragraphs, and in abbreviated form on associated Service Sheets. A thorough understanding and use of these aids will greatly assist the technician in the location of faults.

8-239. Power-Up Self Check

8-240. The HP 5005A, upon power-up, performs a series of self-tests which exercise a sampling of internal circuitry. Detected circuit failures or calibration errors may result in the display of a number ERROR message. The numbered ERROR messages correspond to associated circuitry as listed in *Table 8-6*. Although the power-up test is not a 100% validation of the circuits performance, it does provide a fast, convenient method of establishing a level of confidence. Successful completion of the Power-Up Self Check is indicated by a display of four bars (— — — —), with the instrument in the NORM Signature Analysis mode. Refer to paragraph 3-27.

Table 8-6. Error Messages

ERROR	DESCRIPTION	ASSOCIATED ASSEMBLY
Err00	ROM checksum error.	A3
Err 01-03	Not Assigned.	
Err04	RAM read/write error.	A3
Err05	Not Assigned.	
Err06	Timer error.	A3
Err07	DVM/Ohmmeter Zero Offset exceeds +−00200.	A2
Err08	DVM data exceeds 32000.	A2
Err09	DVM 10v calibration measurement on 25v range exceeds 10.3v.	A2
Err10	DVM 10v calibration measurement on 25v range is less than 9.3 v.	A2
Err11	DVM 10v calibration measurement on 250v range exceeds 10.3v.	A2
Err12	DVM 10v calibration measurement on 250v range is less than 9.3v.	A2
Err13	OHMS 2v calibration exceeds 2.1v.	A2
Err14	OHMS 2v calibration is less than 1.9v.	A2
Err15	Internal count test or keyboard error.	A1
Err16	DAC Zero Offset exceeded 200mv.	A1
Err18	DVM measurement timeout: M/Z status incorrect.	A1/A2
Err19	DVM data transfer error: digit strobe status incorrect.	A1/A2
Err20	Keyboard error: Keyboard encoder DATA VALID signal error.	A1/A4

8-241. The power-up self test performed by the instrument can be divided into seven subsections. They are:

- ROM test
- RAM test
- Timer test
- DVM test
- Partial DAC test
- Internal Count test
- LED test

a. ROM Test

Associated Error Messages: Err00 ROM checksum error.

The ROM test does an arithmetic computation which uses all the words stored in Read Only Memory as addends. The microprocessor computes an arithmetic sum and compares this sum to a previously computed (by the designer) sum stored in ROM. If the two results are not equal the 5005A attempts to display Err00.

b. RAM Test

Associated Error Messages: Err04 RAM read/write error.

The RAM test writes the low order address byte of the addressed byte into the addressed byte (address as data). This is performed on all 256 RAM locations. The 256 locations are then read from and the contents are compared to the original data stored there. The complement of the original data is then stored in each location and read for comparison. If either test fails (i.e. the read byte does not equal the written byte), the 5005A attempts to display Err04.

c. Timer Test

Associated Error Messages: Err06 Timer error.

The Timer test exercises the timer and its associated flip-flop and microprocessor interrupt. A gross comparison of timer accuracy to the cycle time of the microprocessor is performed. If either circuit fails the 5005A attempts to display Err06.

d. DVM Test

Associated Error Messages: Err07 DVM or Ohmmeter Zero Offset exceeds ±00200.

Err08 DVM data exceeds 32000.
Err09 DVM 10V calibration measurement on 25V range exceeds 10.3V.
Err10 DVM 10V calibration measurement on 25V range is less than 9.3V.
Err11 DVM 10V calibration measurement on 250V range exceeds 10.3V.
Err12 DVM 10V calibration measurement on 250V range is less than 9.3V.
Err13 OHMS 2V calibration exceeds 2.1V.
Err14 OHMS 2V calibration is less than 1.9V.
Err18 DVM measurement timeout (M/Z status incorrect).
Err19 DVM data transfer error (digit strobe status incorrect).

The DVM test performs many measurements. The first is a test of the functions associated with the DVM IC's U4 and U7, including the Zero Offset. If the results fall outside a preset range the 5005A attempts to display Err07. If the accumulated data exceeds 32000 counts, the 5005A will attempt to display Err08.

If Zero Offset passes, the 5005A attempts an auto calibration routine. If the calibration voltage (nominally 10.0V) falls outside a preset limit (as described in Err09-Err12), the 5005A attempts to display the appropriate message.

The 2.0 Volt reference associated with the Ohmmeter circuitry is checked next. If it falls out of a preset range (described in Err13 and Err14) the 5005A attempts to display Err13 or Err14.

The 5005A will attempt to display Err18 if the M/Z status bit of U7 (on the DVM board) does not go low to indicate a data transfer within the proper time frame. The 5005A will attempt to display Err19 if a strobe pulse does not occur within the proper time frame.

e. Partial DAC Test

Associated Error Messages: Err16 DAC Zero Offset exceeded 200mv.

This test checks two of the four DAC's on the Main Assembly. DACs U1 and U4 are addressed and tested. If either output exceeds 200 mv, the 5005A attempts to display Err16.

f. Internal Count Test

Associated Error Messages: Err 15 Internal Count Test.

During this test, the internal 10MHz clock is routed to the internal counter and a check is made of the counter circuits. Much of the Signature Analysis circuitry is verified by this test. If the normal output from this test is not found, the 5005A attempts to display Err15.

g. LED Test

Associated Error Messages: None

The LED test lights all the front panel LEDs, digit segments, and decimal points, except "GATE" and "UNSTABLE". The GATE and UNSTABLE LEDs should flash on momentarily during the cycle and therefore can be checked for operation. The operator must verify that all of the LEDs are functioning properly. An unlighted LED or LED segment indicates a bad device.

8-242. Built-in Diagnostics

8-243. The 5005A provides twenty eight user-activated Diagnostic troubleshooting routines, selectable through the two rotary switches (S1 and S2) on the A1 Main Assembly. All tests are initiated by setting the rotary switches to the appropriate switch codes and then turning the LINE switch to OFF and then back to ON. A new test may not be initiated except by this power-down/power-up sequence. *Table 8-7* lists the test switch codes and explains each test.

8-244. It should be noted that the majority of these tests are intended to be used only after the operation of the kernel has been sucessfully verified. The initial Power-Up Self Check will tell much about the status of the kernel. Referring to the Overall Troubleshooting Flowchart, any Power-Up indication, with the exception of Blank/Hieroglyphics or Error Message 00, generally indicates the kernel is functioning properly. Such symptoms allow the technician to logically bypass the extensive kernel Diagnostics, and proceed to a suspect assembly, where the local Diagnostic Procedures can be performed.

Table 8-7. Diagnostic Switch Codes

SWITCH CODE		TEST DESCRIPTION	ASSOCIATED ASSEMBLY
SW1	SW2		
0	0	Normal operation.	
0	1	ROM diagnostic, SA compatible.	KERNEL/A3
0	2	Not assigned.	
0	3	RAM diagnostic, SA compatible.	A3
0	4	I/O diagnostic, SA compatible.	A3
0	5	Timer test.	A3
0	6	Signature analysis circuit diagnostic, SA compatible.	A1
0	7	Count diagnostic, SA compatible.	A1
0	8	Time interval diagnostic, SA compatible.	A1
		*** Tests 09 to 0C test the DAC voltage levels referenced to the 5005A inputs. ***	
		DAC U1 DAC U4 DAC U7 DAC U13	
0	9	0.0V 12.75V 750MV −12.75V	A1
0	A	12.75V 750MV −12.75V 0.0V	A1
0	B	750MV −12.75V 0.0V 12.75V	A1
0	C	−12.75V 0.0V 12.75V 750MV	A1
0	D	DAC ramp exercise: Programs all DACs to cycle from −12.75V to +12.75V in a repetitive ramp function.	A1
0	E	Display the VP+ Zero Offset value.	A1
0	F	Display the VP− Zero Offset value.	A1
1	0	Display the DVM Zero Offset value for the 25V range.	A2
1	1	Display the DVM AUTO-CAL value for the 25V range.	A2
1	2	Display the uncorrected DVM reading for the 25V range.	A2
1	3	Display the DVM Zero Offset value for the 250V range.	A2
1	4	Display the DVM AUTO-CAL value for the 250V range.	A2
1	5	Display the uncorrected DVM reading for the 250V range.	A2
1	6	Display the Zero Offset value for OHMS.	A2
1	7	Display the reference voltage for OHMS.	A2
1	8	Display the measured voltage for OHMS.	A2
1	9	Turn on all LEDs and display segments, and flash the "GATE" and "UNSTABLE" LEDs.	A4
1	A	Display a shifting pattern of all characters normally displayed.	A4
1	B	Display the "key code" of the last key depressed.	A4
2	(X)	Free Run: Force an aborted read of all memory content.	KERNEL

(X = don't care)

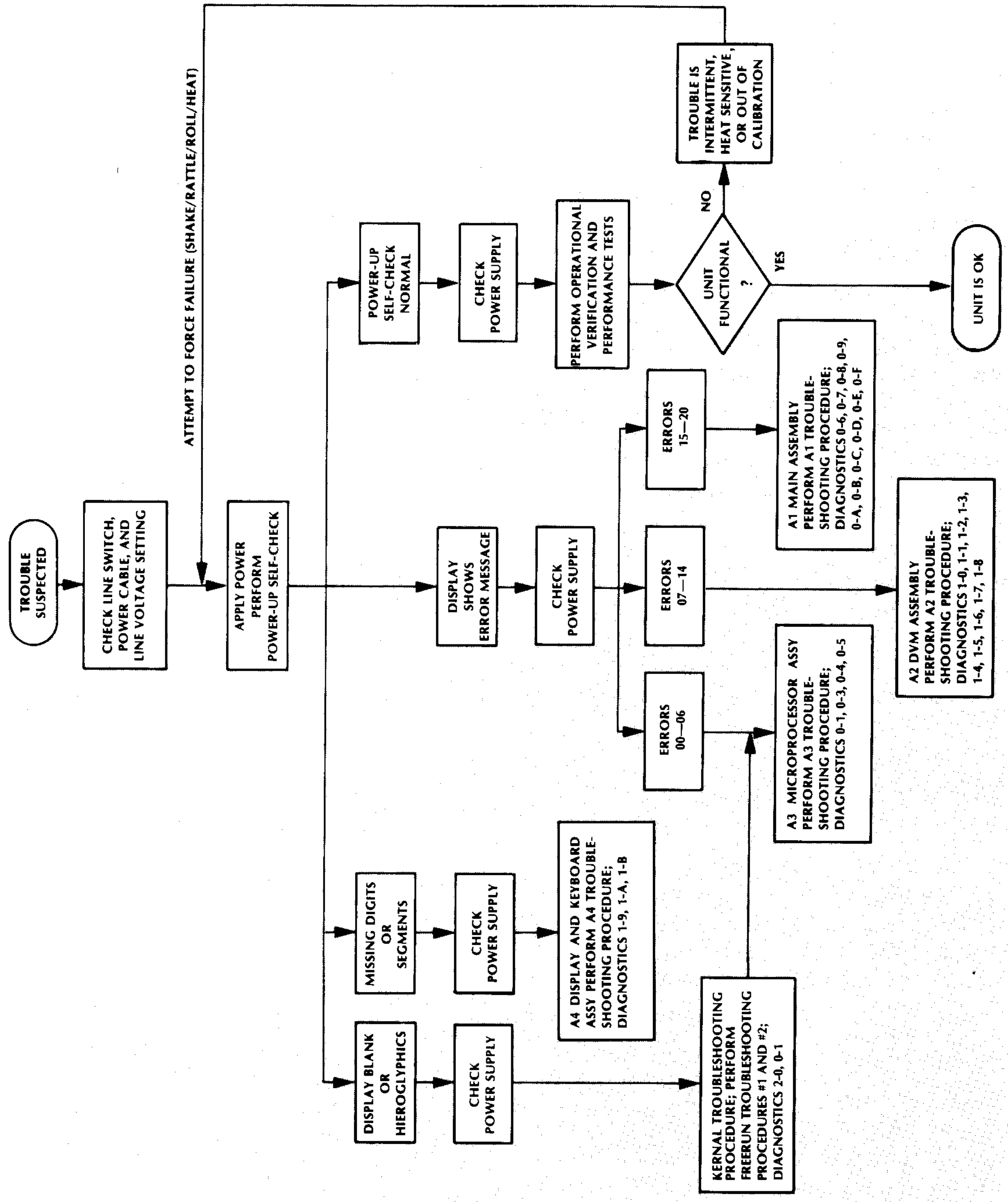

TROUBLE SUSPECTED
CHECK LINE SWITCH, POWER CABLE, AND LINE VOLTAGE SETTING
APPLY POWER PERFORM POWER-UP SELF-CHECK
ATTEMPT TO FORCE FAILURE (SHAKE/RATTLE/ROLL/HEAT)
POWER-UP SELF-CHECK NORMAL
CHECK POWER SUPPLY
PERFORM OPERATIONAL VERIFICATION AND PERFORMANCE TESTS
UNIT FUNCTIONAL ?
NO
TROUBLE IS INTERMITTENT, HEAT SENSITIVE, OR OUT OF CALIBRATION
YES
UNIT IS OK
DISPLAY SHOWS ERROR MESSAGE
CHECK POWER SUPPLY
ERRORS 15—20
A1 MAIN ASSEMBLY PERFORM A1 TROUBLE-SHOOTING PROCEDURE; DIAGNOSTICS 0-6, 0-7, 0-8, 0-9, 0-A, 0-B, 0-C, 0-D, 0-E, 0-F
ERRORS 07—14
A2 DVM ASSEMBLY PERFORM A2 TROUBLE-SHOOTING PROCEDURE; DIAGNOSTICS 1-0, 1-1, 1-2, 1-3, 1-4, 1-5, 1-6, 1-7, 1-8
ERRORS 00—06
A3 MICROPROCESSOR ASSY PERFORM A3 TROUBLE-SHOOTING PROCEDURE; DIAGNOSTICS 0-1, 0-3, 0-4, 0-5
MISSING DIGITS OR SEGMENTS
CHECK POWER SUPPLY
A4 DISPLAY AND KEYBOARD ASSY PERFORM A4 TROUBLE-SHOOTING PROCEDURE; DIAGNOSTICS 1-9, 1-A, 1-B
DISPLAY BLANK OR HIEROGLYPHICS
CHECK POWER SUPPLY
KERNAL TROUBLESHOOTING PROCEDURE; PERFORM FREERUN TROUBLESHOOTING PROCEDURES #1 AND #2; DIAGNOSTICS 2-0, 0-1

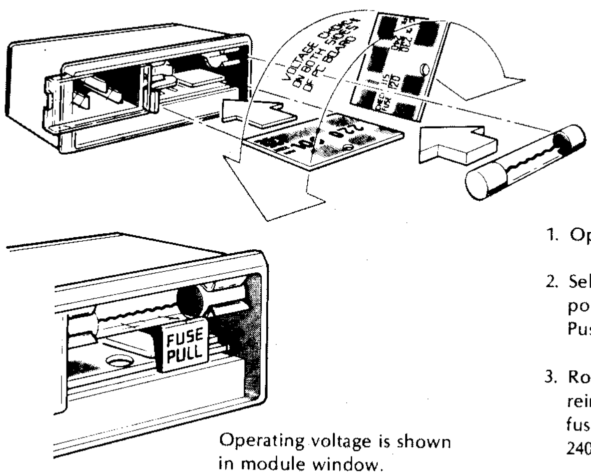
Figure 8-14. Overall Troubleshooting Flowchart

8-245. OVERALL TROUBLESHOOTING

8-246. All troubleshooting initiates with the Power-Up Self Check. In general, the Power-Up Self Check will produce one of four types of display; a blank or hieroglyphic display, a numbered Error message, a display with missing digits or segments, or a normal indication (four bars). The Overall Troubleshooting Flowchart illustrates the potential fault areas associated with each type of display. The technician should follow the flowchart procedure to identify the faulty assembly. Once the faulty assembly is isolated, the technician can proceed directly to the corresponding Service Sheet. The Service Sheet contains the schematic diagram, block diagram, component locator, associated Error messages, and abbreviated Diagnostic procedures.

8-247. The following procedure describes the recommended preliminary troubleshooting, and references the Overall Troubleshooting Flowchart in *Figure 8-14.*

a. Insure that the line voltage programming card is properly inserted for the intended line voltage. This card is located beneath the line fuse in the A7 Line Module. Hold the card so that proper voltage range can be read normally and place the top of the card first into the instrument. See *Figure 8-15.*



Operating voltage is shown in module window.

SELECTION OF OPERATING VOLTAGE

1. Open cover door and rotate fuse-pull to left.
2. Select operating voltage by orienting PC board to position desired voltage on top-left side. Push board firmly into module slot.
3. Rotate fuse-pull back into normal position and reinsert fuse in holders, using caution to select correct fuse value. (0.25A Slow Blow/250V for 220V and 240V and 0.50A for 100V and 120V.

Figure 8-15. Line Voltage Selection

b. Connect the main power cable to the 5005A. Set the LINE switch to the ON position.

c. Observe the Display. The 5005A should immediately perform the Power-Up Self Check, (see paragraph 8-239), terminating in the NORM Signature analysis Mode. If a trouble exists, the operator should observe one of the following display responses:

   1. Display Blank or Hieroglyphics. The display presents meaningless hieroglyphics or random segments, or no display at all.
   2. Display Shows Error Messages. The display provides a numbered Error Message.
   3. Missing Digits or Segments. One or more digits or segments in a digit do not light, but a legible non-intermittent display is visible.
   4. Power-Up Self Check Normal. The power-up routine (see paragraph 3-27) appears normal. The instrument displays four bars (— — — —) and assumes the NORM Signature Analysis mode.

d. For all failure indications, it is always recommended that the instruments internal power supplies be checked first. The 5005A power supply contains four dc supplies; +5 volts, -5.2 volts, +12 volts, -12 volts. These supplies are generated on the A1 Main Assembly, and are labeled in several locations. Measure each supply. If any supply appears low or high, refer to Power Supply Troubleshooting, Paragraph 8-248.

e. Display response (1.) indicates the trouble may be associated with the kernel. Perform the Kernel Troubleshooting Procedure, paragraph 8-256.

f. Display response (2.) is an indication that the kernel is functioning properly and that, in general, only the circuitry associated with the indicated error message need be checked. Refer to the Overall Troubleshooting Flowchart, *Figure 8-14,* for specific assembly procedures.

g. The probable cause of display response (3.) is an isolated faulty LED digit, or the associated digit driver circuit.

h. Display response (4.) could indicate the unit is operating properly and there is no trouble, or an intermittent, heat sensitive or calibration failure. Confirm by performing the Operation Verification and/or Performance Tests, and then attempt to force the suspect failure appear.

WARNING

All troubleshooting procedures require internal access to the instrument with the protective covers removed. These procedures should be performed only by service-trained personnel who are aware of the hazards involved.

NOTE

To access the internal circuitry for the Timing Pod, Data Probe, or Main Instrument, refer to the Disassembly Procedures in paragraph 8-62.

8-248. POWER SUPPLY TROUBLESHOOTING

8-249. Remove the top cover of the instrument. If necessary, refer to the Disassembly and Reassembly procedures beginning with paragraph 8-62. Connect the main power cable, and set the LINE switch to ON. After the Power-Up Self Check routine is completed, measure the four dc voltages on the A1 Main Assembly using a digital voltmeter. The measurement locations are indicated in *Figure 8-16.* Verify that the measured voltages are within the tolerances listed below. If any supply is incorrect, review the following paragraphs. The proper voltages appearing at the power supply outputs are:

+5 volts D.C. + or - 0.25 volts
+12 volts D.C. + or - 0.6 volts
-12 volts D.C. + or - 0.6 volts
-5.2 volts D.C. + or - 0.26 volts

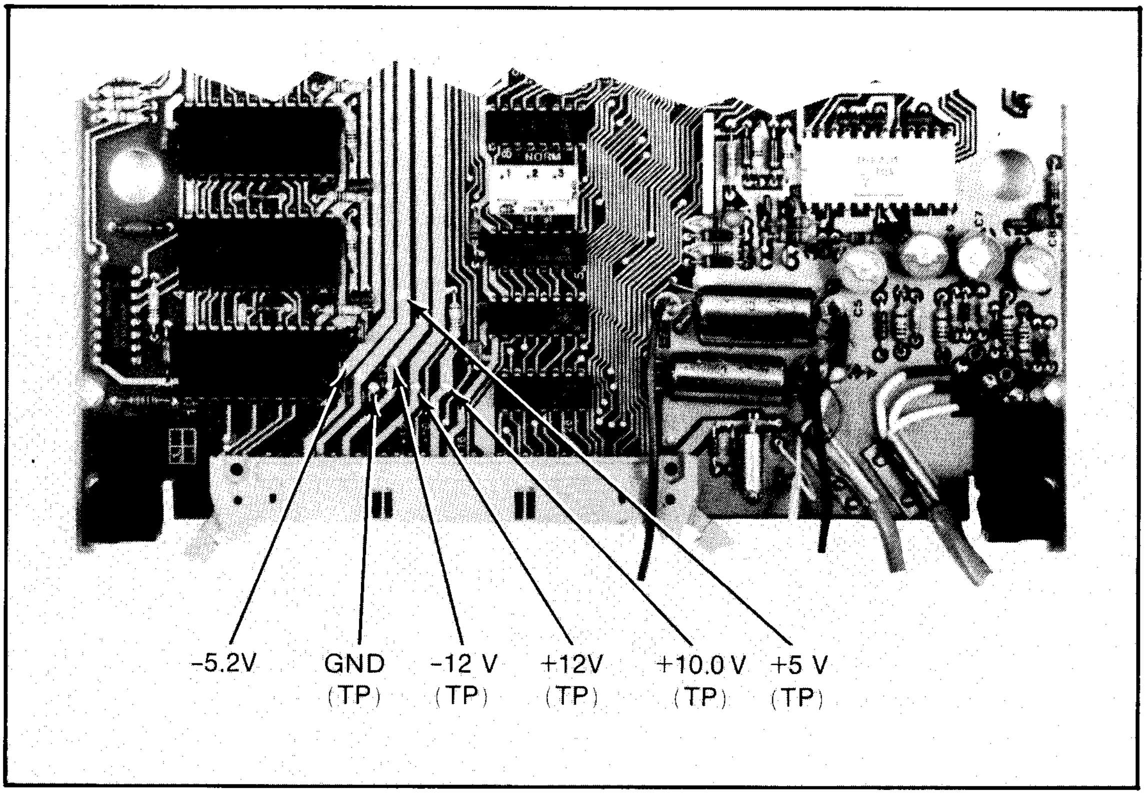

-5.2V
GND (TP)
-12 V (TP)
+12V (TP)
+10.0 V (TP)
+5 V (TP)

Figure 8-16. Power Supply Measurement Locations

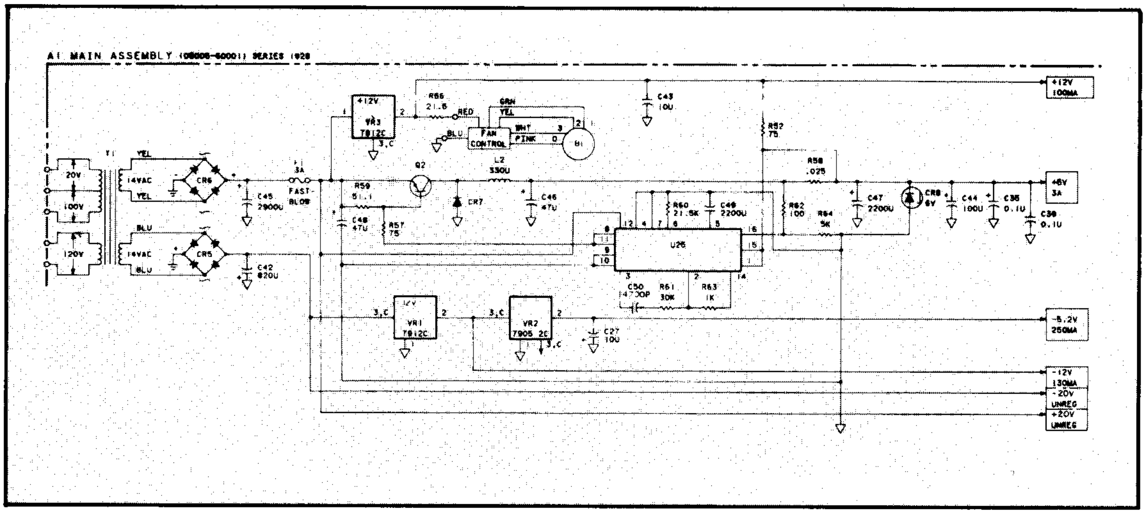
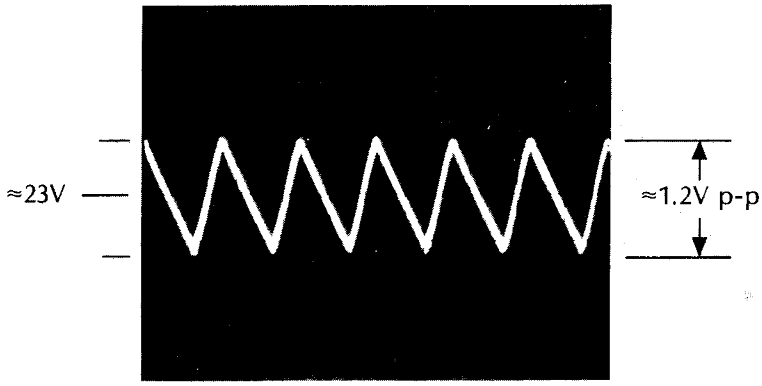

A1 MAIN ASSEMBLY (05005-60001) SERIES 1920
T1
20V
100V
120V
YEL
14VAC
BLU
CR6
CR5
C45 2900U
C42 820U
F1 3A FAST-BLOW
+12V VR3 7812C
3,C
R56 21.6
RED
GRN
YEL
BLU
FAN CONTROL
WHT
PINK
B1
Q2
R59 51.1
C48 47U
R57 75
CR7
L2 330U
C46 47U
C43 10U
R52 75
R58 .025
R60 21.5K
C49 2200U
U26
C50 14700P
R61 30K
R63 1K
R62 100
R64 5K
C47 2200U
CR8 6V
C44 100U
C35 0.1U
C39 0.1U
+12V 100MA
+5V 3A
12V VR1 7912C
VR2 7905 2C
C27 10U
-5.2V 250MA
-12V 130MA
-20V UNREG
+20V UNREG

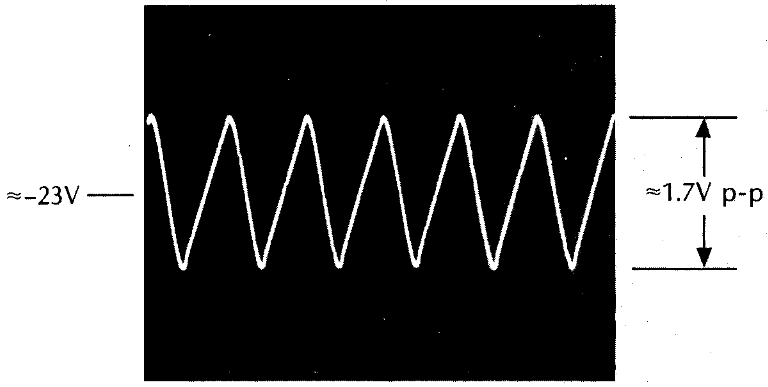
Figure 8-17. 5005A Power Supply

8-250. Refer to the schematic diagram in *Figure 8-17*. The positive dc supplies, +5 V and +12 V, derive their input from bridge rectifier CR6. The negative dc supplies, -5.2 V and -12 V, derive their input from bridge rectifier CR5. The output from the positive rectifier is protected by a three amp fast blow fuse, F1. If the positive supplies are dead, check this fuse and replace if necessary, with HP Part #2110-0003. The main line fuse, within A7, is a half-amp slow blow, HP Part #2110-0202, for the 100 volt settings, or a one-quarter amp slow blow, HP Part #2110-0201, for the 200 volt settings. Measure the output from the rectifiers with an oscilloscope, and compare the waveforms to *Figure 8-18*.



Volts/Div	.05
Time/Div	5 ms
Coupling ...	AC
Probe	10:1

+20 volts unregulated for CR6 (positive output)



Volts/Div	.05
Time/Div	5 ms
Coupling ...	AC
Probe	10:1

-20 volts unregulated for CR5 (negative output)

Figure 8-18. Power Supply Unregulated Supplies

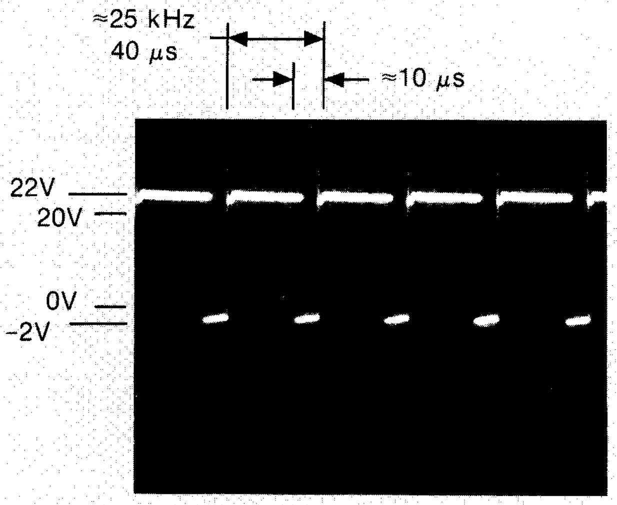
8-251. Three of the four regulated outputs are provided by three-pin series regulators; -12 V by VR1, -5.2 V by VR2, and +12 V by VR3. The +5 volt supply is regulated by a special switching regulator consisting of a pulse width modulation controller U25, and associated circuitry. If the input voltage to regulators is correct and any outputs are incorrect, the regulators are the probable cause (excluding the U25). If replacement of a regulator does not correct the problem, it could be caused by a shorted bypass capacitor or a bad IC. An HP 547A current tracer used in conjunction with an HP 546A logic pulser can be helpful to find the bad component.

8-252. Five Volt Supply

8-253. The five volt regulated power supply uses a switching regulator circuit. The heart of this circuit is a TL494 pulse width modulation controller. The TL494 IC constantly compares the five volt output to its internal five volt reference, using the difference signal to determine the duty cycle of the switching transistor Q2. The supply is current limited to a nominal 4 amps to pin 16 of the TL494, which is compared to pin 15. When the signals are equal (implying that the voltage drop across R58 and R62 are equal) the pulse circuit current-limits the output to 4 amps.

8-254. Diode CR8 is an over voltage protection diode limiting the output to six volts (6 volts). Resistor R52 is used to eliminate start-up problems associated with pin 1 falling below ground. On start-up R52 keeps pin 1 and 15 of U25 (TL494) above ground. Inductor L2 is the primary energy storage device and diode CR7 provides a current path when Q2 is shutoff.

8-255. To check the operation of U25, observe the pulsed output on pin 8. It should be a ≈10 microsecond pulse train, at a 25 kHz rate, with an amplitude of ≈ 20 volts p-p. Refer to the waveform in *Figure 8-19.*



Volts/Div. 1
Time/Div. ... 20 μs
Coupling ..... DC
Probe 10:1

Figure 8-19. A1U25 Switching Output

8-256. KERNEL TROUBLESHOOTING

8-257. The kernel of the instrument is defined to be the power supply and the microprocessor, with its support circuitry, which comprise the minimum required logic circuitry for the 5005A's normal central processing operation.

8-258. Is the Kernel Functional?

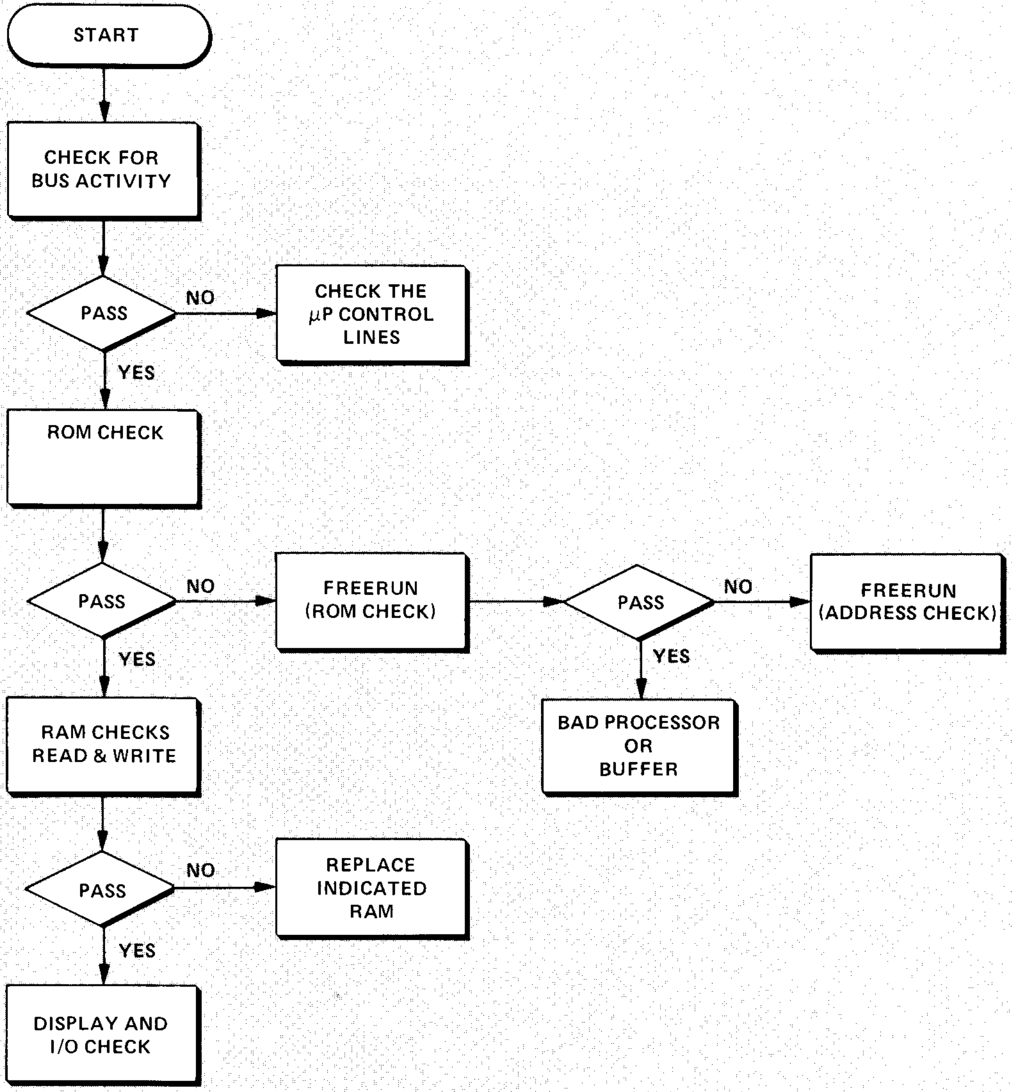
8-259. It is important to remember that all the Diagnostic routines, except Freerun (2-0), require that the kernel of the instrument be working properly. As the procedure for verification of the kernel is extensive, it is helpful to determine its status first. If the kernel can be determined to be working, the technician can proceed directly to an indicated assembly troubleshooting procedure. If, however, the initial symptoms indicate the kernel may be faulty, the technician should perform the following procedure.

8-260. Referring to the Overall Troubleshooting Flowchart, many of the initial turn-on symptoms can indicate whether the kernel is functioning or not. Error Messages, Missing Digits or Segments, or a Normal (four bars) Power-Up Self Check display are logical responses, and generally indicate the kernel is functional. For these types of symptoms the technician should bypass the Kernel troubleshooting, and proceed to an assembly procedure indicated by the flowchart. If a Blank or Hieroglyphic display appears, the operation of the kernel should be suspected. After the power supply is checked, perform the following troubleshooting tests:

Troubleshooting Test	**Diagnostic Number**
Bus Activity Test	—
ROM Test	0-1
RAM Read Test	0-3
RAM Write Test	0-3
Front Panel Activity Test	—
Freerun ROM Test	2-0
Freerun Address Test	2-0

Table 8-8. Kernal Troubleshooting Procedure

The following flowchart illustrates the recommended procedure for troubleshooting the kernel.


START
CHECK FOR BUS ACTIVITY
PASS
NO
CHECK THE µP CONTROL LINES
YES
ROM CHECK
PASS
NO
FREERUN (ROM CHECK)
PASS
NO
FREERUN (ADDRESS CHECK)
YES
BAD PROCESSOR OR BUFFER
YES
RAM CHECKS READ & WRITE
PASS
NO
REPLACE INDICATED RAM
YES
DISPLAY AND I/O CHECK

1. Perform the Bus Activity test.

Purpose: The purpose of this test is to determine if the microprocessor has been halted by some external or internal fault condition.

Procedure:

a. Place a logic probe on the low order bit (AD0) of the microprocessor address bus (pin 12 of U16). A flashing probe indicates there is activity on the bus. If so, the bus is not halted. Proceed to step 3.

b. A static high or low indicates that the microprocessor is being held up by some fault. Check the control lines of the microprocessor listed below, for normal activity. An explanation of the control lines is provided in paragraph 8-209.

Table 8-8. Kernel Troubleshooting Procedure (Continued)

Signal Name	Pin #	Normal Activity
1. READY	35	A non-fixed duty cycle square wave (TTL levels).
2. RST 5.5	9	logic zero (0 volts).
3. RST 6.5	8	logic zero (0 volts).
4. RST 7.5	7	logic one (+5 volts).
5. RESET IN*	36	Goes low on power-up and then goes high.
6. X1	1	5 MHz square wave.
7. X2	2	5 MHz square wave.

(* INDICATES A NEGATED SIGNAL)

Indications:

If the control lines all appear correct, there is a possibility that a bus buffer or other device could be holding the AD0 line. Check other Address lines/Data lines AD1 through AD15 for activity.

2. Perform the ROM test (Diag 0-1).

Purpose: The ROM test is an actual diagnostic program that verifies the microprocessor is running. The ROM test verifies that the microprocessor is actually receiving correct data from the ROM and that it can run a small program. This test also verifies proper operation of buffer U14.

Procedure:

a. Set the diagnostic rotary switches on A3 to 0-1 (S1=0 S2=1).

b. Connect the test signature analyzer as follows:

Controls

START .... Falling edge
STOP .... Rising edge
CLOCK .... Rising edge

Timing Pod

START .... A3 TP A15
STOP .... A3 TP A15
CLOCK .... A3 TP $\overline{\text{RD}}$
GND .... A3 TP GND

c. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

Table 8-8. Kernel Troubleshooting Procedure (Continued)

d. Verify the signatures for A3 U16, shown below.

S.A. Setup — Polarities

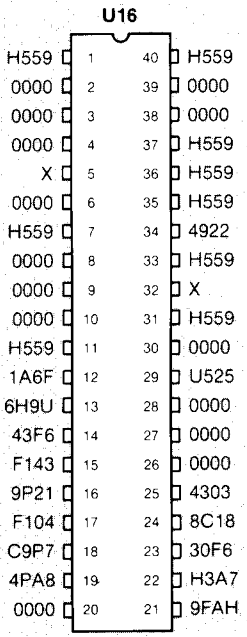
Clk: ↑
Start: ↓
Stop: ↑

S.A. Setup — UUT Connections

Clk: $\overline{RD}$
Start/Stop: A15
Stop Qual: A15

Vcc **Signature = H559**

"X" Signature = Don't Care


U16
H559 1
0000 2
0000 3
0000 4
X 5
0000 6
H559 7
0000 8
0000 9
0000 10
H559 11
1A6F 12
6H9U 13
43F6 14
F143 15
9P21 16
F104 17
C9P7 18
4PA8 19
0000 20
40 H559
39 0000
38 0000
37 H559
36 H559
35 H559
34 4922
33 H559
32 X
31 H559
30 0000
29 U525
28 0000
27 0000
26 0000
25 4303
24 8C18
23 30F6
22 H3A7
21 9FAH

Indications:

If the signatures are correct, continue with the RAM read test in step 3. If any of the signatures are incorrect, proceed to Freerun checks, beginning with step 6.

3. Perform RAM Read Test (Diag 0-3).

Purpose: The following test verifies that the RAM is capable of being written-to and read-from. If the given signatures are incorrect, perform the RAM Write test to verify that a proper write is being performed on the RAM. The RAM write test should logically separate a write or control problem from a read problem.

Table 8-8. Kernel Troubleshooting Procedure (Continued)

Procedure:

a. Set the diagnostic rotary switches on A3 to 0-3 (S1=0 S2=3).

b. Connect the test signature analyzer as follows:

Controls

START	Falling edge
STOP	Rising edge
CLOCK	Rising edge

Timing Pod

START	A3 TP A15
STOP	A3 TP A15
CLOCK	A3 TP $\overline{\text{RD}}$
GND	A3 TP GND

c. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

d. Verify the signatures for A3 U16 and U8, shown below.

S.A. Setup — Polarities

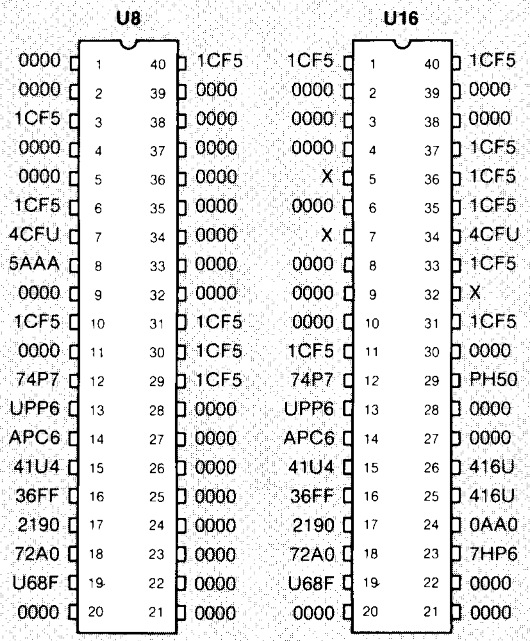
Clk: ↑
Start: ↓
Stop: ↑

S.A. Setup — UUT Connections

Clk: $\overline{\text{RD}}$
Start/Stop: A15
Stop Qual: A15

Vcc **Signature = 1CF5**

"X" Signature = Don't Care



Pin	U8	U16
1	0000	1CF5
2	0000	0000
3	1CF5	0000
4	0000	0000
5	0000	X
6	1CF5	0000
7	4CFU	X
8	5AAA	0000
9	0000	0000
10	1CF5	0000
11	0000	1CF5
12	74P7	74P7
13	UPP6	UPP6
14	APC6	APC6
15	41U4	41U4
16	36FF	36FF
17	2190	2190
18	72A0	72A0
19	U68F	U68F
20	0000	0000
21	0000	0000
22	0000	0000
23	0000	7HP6
24	0000	0AA0
25	0000	416U
26	0000	416U
27	0000	0000
28	0000	0000
29	1CF5	PH50
30	1CF5	0000
31	1CF5	1CF5
32	0000	X
33	0000	1CF5
34	0000	4CFU
35	0000	1CF5
36	0000	1CF5
37	0000	1CF5
38	0000	0000
39	0000	0000
40	1CF5	1CF5

Table 8-8. Kernel Troubleshooting Procedure (Continued)

Indications:

If the given signatures are correct, the RAM is verified. Proceed to step 5. If the given signatures are incorrect, perform the RAM Write test to verify that a proper write is being performed on the RAM. The RAM Write test should logically separate a write or control problem from a read problem.

4. Perform RAM Write Test (Diag 0-3).

NOTE

> This test is not necessary if the previous RAM read test performs properly.

Purpose: This test performs the same test as RAM Read but allows signatures to be taken of the Data lines when a write occurs.

Procedure:

a. Set the diagnostic rotary switches on A3 to 0-3 (S1=0 S2=3).

b. Connect the test signature analyzer as follows:

Controls

START	Falling edge
STOP	Rising edge
CLOCK	Rising edge

Timing Pod

START	A3 TP A15
STOP	A3 TP A15
CLOCK	A3 TP $\overline{WR}$
GND	A3 TP GND

c. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

d. Verify the signatures for A3 U16 and U8, shown below.

S.A. Setup — Polarities

Clk: ↑
Start: ↓
Stop: ↑

S.A. Setup — UUT Connections

Clk: $\overline{WR}$
Start/Stop: A15
Stop Qual: A15

Vcc **Signature = 4596**

"X" Signature = Don't Care

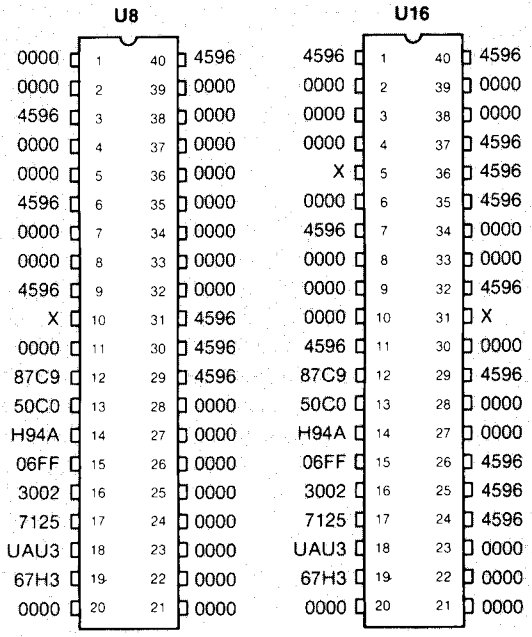

U8
0000 1 40 4596
0000 2 39 0000
4596 3 38 0000
0000 4 37 0000
0000 5 36 0000
4596 6 35 0000
0000 7 34 0000
0000 8 33 0000
4596 9 32 0000
X 10 31 4596
0000 11 30 4596
87C9 12 29 4596
50C0 13 28 0000
H94A 14 27 0000
06FF 15 26 0000
3002 16 25 0000
7125 17 24 0000
UAU3 18 23 0000
67H3 19 22 0000
0000 20 21 0000
U16
4596 1 40 4596
0000 2 39 0000
0000 3 38 0000
0000 4 37 4596
X 5 36 4596
0000 6 35 4596
4596 7 34 0000
0000 8 33 0000
0000 9 32 4596
0000 10 31 X
4596 11 30 0000
87C9 12 29 4596
50C0 13 28 0000
H94A 14 27 0000
06FF 15 26 4596
3002 16 25 4596
7125 17 24 4596
UAU3 18 23 0000
67H3 19 22 0000
0000 20 21 0000

Table 8-8. *Kernel Troubleshooting Procedure (Continued)*

Indications:

If any of the given signatures are incorrect, suspect a bad RAM. Check for activity on the control lines; $\overline{WR}$, $\overline{CE}$, $\overline{RD}$, and IO/$\overline{M}$.

5. Check the front panel Display for activity.

Purpose: The purpose of this test is to verify that the front panel Display is responding to the Display Decoder Driver.

Procedure:

a. To test for activity on the front panel display, turn the UUT to on. There should be some kind of illuminated display present. Place a logic probe on the "a through g, dp, and 1 through 8" outputs of A3U6, the Display Decoder Driver.

b. Verify that the logic probe flashes, indicating activity, on each of the lines.

Indications:

If there is bus activity, and there are no segments lighted, suspect a bad ribbon cable or open/shorted VCC lines on A4. No bus activity indicates A3U6 is faulty. Retrace the inputs for A3U6.

6. Perform the Freerun ROM test (Diag 2-0).

Purpose: The purpose of the procedure is to verify the contents of all three ROMs, and data bus buffer U14.

Procedure:

a. Set the diagnostic rotary switches on A3 to 2-0 (S1=2 S2=0).

b. Connect the test signature analyzer as follows:

Controls

START	Falling edge
STOP	Rising edge
CLOCK	Rising edge

Timing Pod

START	A3 TP CE1
STOP	A3 TP CE3
CLOCK	A3 TP $\overline{RD}$
GND	A3 TP GND

c. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

d. Verify the signatures for A3 U4, shown below. If all appear correct, the contents of all the ROMs is verified. If any signatures are incorrect, first verify that the freerun pattern has been forced onto the bus by the microprocessor. Check the signatures at A3 U16. If U16 signatures are correct, one of the three ROMs is bad. To determine which ROM is bad, continue procedure.

Table 8-8. Kernel Troubleshooting Procedure (Continued)

S.A. Setup — Polarities

Clk: ↑
Start: ↓
Stop: ↑

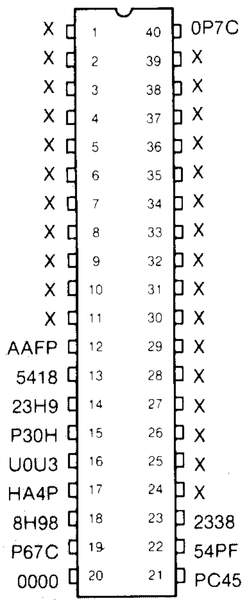
S.A. Setup — UUT Connections

Clk: $\overline{\text{RD}}$
Start/Stop: CE1
Stop Qual: CE3

Vcc **Signature** = **OP7C**

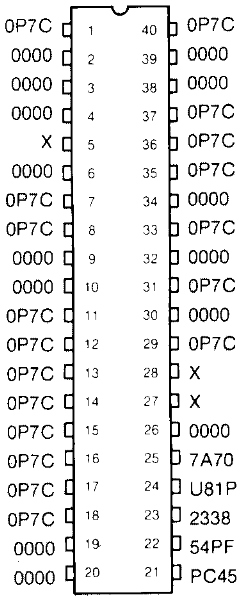
"X" Signature = **Don't Care**

U4



Pin	Signature	Pin	Signature
1	X	40	0P7C
2	X	39	X
3	X	38	X
4	X	37	X
5	X	36	X
6	X	35	X
7	X	34	X
8	X	33	X
9	X	32	X
10	X	31	X
11	X	30	X
12	AAFP	29	X
13	5418	28	X
14	23H9	27	X
15	P30H	26	X
16	U0U3	25	X
17	HA4P	24	X
18	8H98	23	2338
19	P67C	22	54PF
20	0000	21	PC45

U16



Pin	Signature	Pin	Signature
1	0P7C	40	0P7C
2	0000	39	0000
3	0000	38	0000
4	0000	37	0P7C
5	X	36	0P7C
6	0000	35	0P7C
7	0P7C	34	0000
8	0P7C	33	0P7C
9	0000	32	0000
10	0000	31	0P7C
11	0P7C	30	0000
12	0P7C	29	0P7C
13	0P7C	28	X
14	0P7C	27	X
15	0P7C	26	0000
16	0P7C	25	7A70
17	0P7C	24	U81P
18	0P7C	23	2338
19	0000	22	54PF
20	0000	21	PC45

e. To verify the contents of ROM U11, connect the signature analyzer ST and SP lines to CE1 and turn the LINE switch from ON to OFF then back to ON. Verify the following signatures.

S.A. Setup — Polarities

Clk: ↑
Start: ↓
Stop: ↑

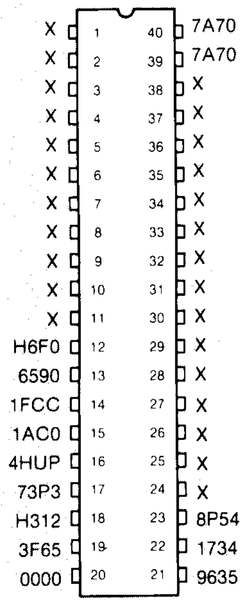
S.A. Setup — UUT Connections

Clk: $\overline{\text{RD}}$
Start/Stop: CE1
Stop Qual: CE1

Vcc **Signature** = **7A70**

"X" Signature = **Don't Care**

U11



Pin	Signature	Pin	Signature
1	X	40	7A70
2	X	39	7A70
3	X	38	X
4	X	37	X
5	X	36	X
6	X	35	X
7	X	34	X
8	X	33	X
9	X	32	X
10	X	31	X
11	X	30	X
12	H6F0	29	X
13	6590	28	X
14	1FCC	27	X
15	1AC0	26	X
16	4HUP	25	X
17	73P3	24	X
18	H312	23	8P54
19	3F65	22	1734
20	0000	21	9635

Table 8-8. Kernel Troubleshooting Procedure (Continued)

f. To verify the contents of ROM U13, connect the signature analyzer ST and SP lines to CE2 and turn the LINE switch from ON to OFF then back to ON. Verify the following signatures.

S.A. Setup — Polarities

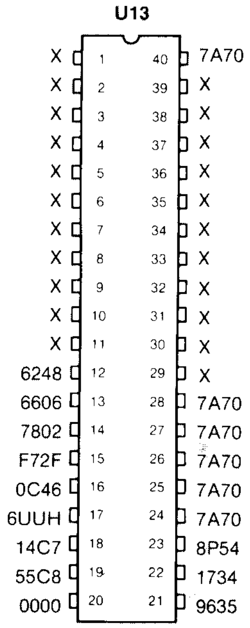
Clk: ↑
Start: ↓
Stop: ↑

S.A. Setup — UUT Connections

Clk: $\overline{\mathrm{RD}}$
Start/Stop: CE2
Stop Qual: CE2

Vcc **Signature = 7A70**

"X" Signature = Don't Care


U13
X 1
X 2
X 3
X 4
X 5
X 6
X 7
X 8
X 9
X 10
X 11
6248 12
6606 13
7802 14
F72F 15
0C46 16
6UUH 17
14C7 18
55C8 19
0000 20
9635 21
1734 22
8P54 23
7A70 24
7A70 25
7A70 26
7A70 27
7A70 28
29 X
30 X
31 X
32 X
33 X
34 X
35 X
36 X
37 X
38 X
39 X
40 7A70

g. To verify the contents of ROM U4, connect the signature analyzer ST and SP lines to CE3 and turn the LINE switch from ON to OFF then back to ON. Verify the following signatures.

S.A. Setup — UUT Connections

Clk: $\overline{\mathrm{RD}}$
Start/Stop: CE3
Stop Qual: CE3

S.A. Setup — Polarities

Clk: ↑
Start: ↓
Stop: ↑

Vcc **Signature = 7A70**

"X" Signature = Don't Care

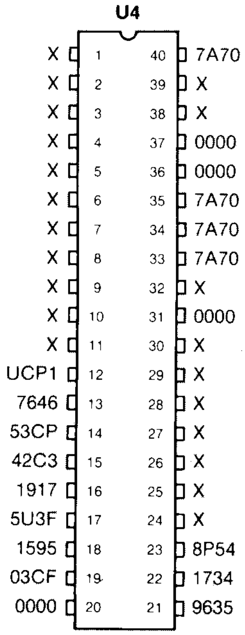

U4
X 1
X 2
X 3
X 4
X 5
X 6
X 7
X 8
X 9
X 10
X 11
UCP1 12
7646 13
53CP 14
42C3 15
1917 16
5U3F 17
1595 18
03CF 19
0000 20
9635 21
1734 22
8P54 23
24 X
25 X
26 X
27 X
28 X
29 X
30 X
31 0000
32 X
33 7A70
34 7A70
35 7A70
36 0000
37 0000
38 X
39 X
40 7A70

Table 8-8. Kernel Troubleshooting Procedure (Continued)

7. Perform the Freerun Address Check (Diag 2-0).

Purpose: The purpose of this test is to verify the address selection and decoding lines from the kernel. It places the microprocessor in a freerun address loop, allowing stable signatures on the kernel outputs.

Procedure:

a. Set the diagnostic rotary switches on A3 to 2-0 (S1=2 S2=0).

b. Connect the test signature analyzer as follows:

Controls

START	Rising edge
STOP	Rising edge
CLOCK	Falling edge

Timing Pod

START	A3 TP A15
STOP	A3 TP A15
CLOCK	A3 TP ALE
GND	A3 TP GND

c. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

d. Verify the signatures for A3 U4, shown below.

S.A. Setup — Polarities

Clk: ↓
Start: ↑
Stop: ↑

S.A. Setup — UUT Connections

Clk: ALE
Start/Stop: A15
Stop Qual: A15

Vcc **Signature** = **0001**

"X" Signature = **Don't Care**

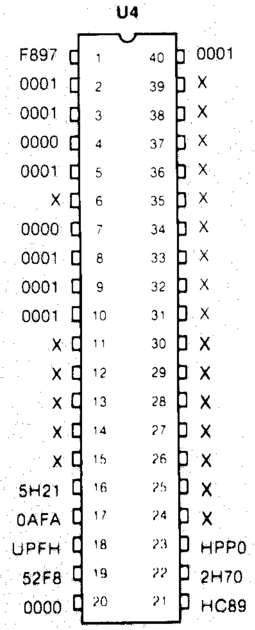
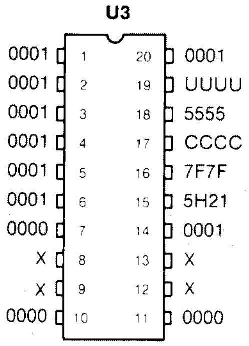
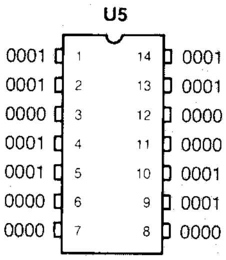

U4
F897 1
0001 2
0001 3
0000 4
0001 5
X 6
0000 7
0001 8
0001 9
0001 10
X 11
X 12
X 13
X 14
X 15
5H21 16
0AFA 17
UPFH 18
52F8 19
0000 20
40 0001
39 X
38 X
37 X
36 X
35 X
34 X
33 X
32 X
31 X
30 X
29 X
28 X
27 X
26 X
25 X
24 X
23 HPP0
22 2H70
21 HC89

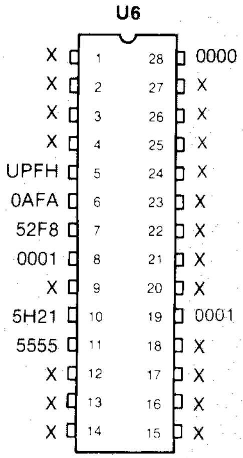
Table 8-8. Kernel Troubleshooting Procedure (Continued)

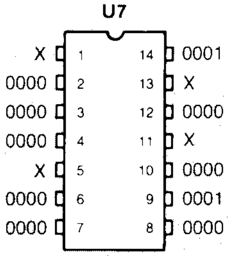
Indications:

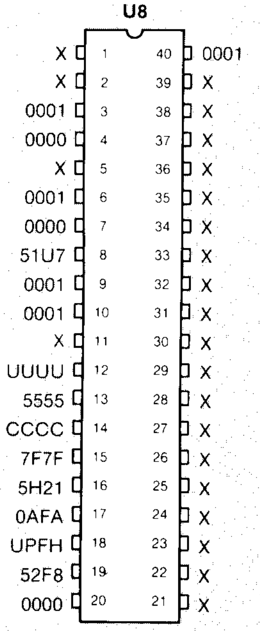
If any of the signatures are incorrect, try to backtrace the faults by taking previous path signatures. A majority of the A3 IC signatures for this diagnostic mode are given below.

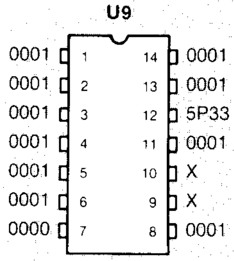

U3
0001 1 20 0001
0001 2 19 UUUU
0001 3 18 5555
0001 4 17 CCCC
0001 5 16 7F7F
0001 6 15 5H21
0000 7 14 0001
X 8 13 X
X 9 12 X
0000 10 11 0000

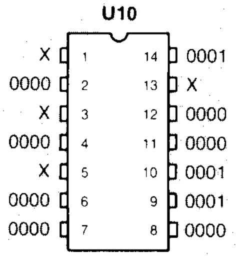

U5
0001 1 14 0001
0001 2 13 0001
0000 3 12 0000
0001 4 11 0000
0001 5 10 0001
0000 6 9 0001
0000 7 8 0000


U6
X 1 28 0000
X 2 27 X
X 3 26 X
X 4 25 X
UPFH 5 24 X
0AFA 6 23 X
52F8 7 22 X
0001 8 21 X
X 9 20 X
5H21 10 19 0001
5555 11 18 X
X 12 17 X
X 13 16 X
X 14 15 X


U7
X 1 14 0001
0000 2 13 X
0000 3 12 0000
0000 4 11 X
X 5 10 0000
0000 6 9 0001
0000 7 8 0000


U8
X 1 40 0001
X 2 39 X
0001 3 38 X
0000 4 37 X
X 5 36 X
0001 6 35 X
0000 7 34 X
51U7 8 33 X
0001 9 32 X
0001 10 31 X
X 11 30 X
UUUU 12 29 X
5555 13 28 X
CCCC 14 27 X
7F7F 15 26 X
5H21 16 25 X
0AFA 17 24 X
UPFH 18 23 X
52F8 19 22 X
0000 20 21 X


U9
0001 1 14 0001
0001 2 13 0001
0001 3 12 5P33
0001 4 11 0001
0001 5 10 X
0001 6 9 X
0000 7 8 0001


U10
X 1 14 0001
0000 2 13 X
X 3 12 0000
0000 4 11 0000
X 5 10 0001
0000 6 9 0001
0000 7 8 0000

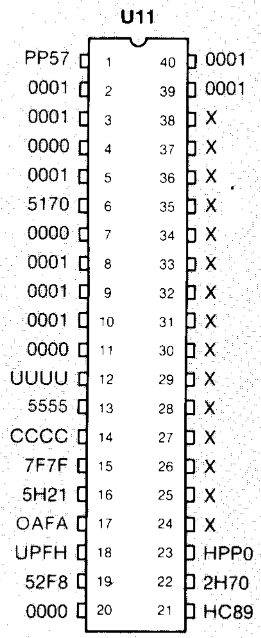
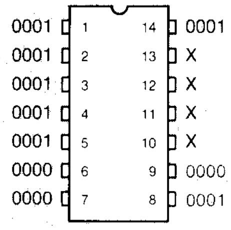
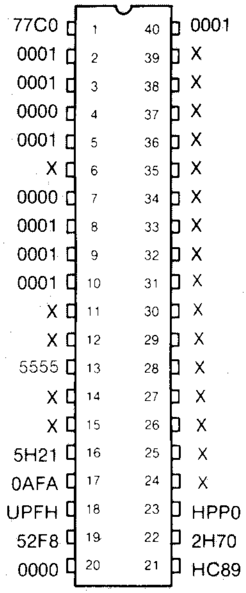

U11
PP57 1 40 0001
0001 2 39 0001
0001 3 38 X
0000 4 37 X
0001 5 36 X
5170 6 35 X
0000 7 34 X
0001 8 33 X
0001 9 32 X
0001 10 31 X
0000 11 30 X
UUUU 12 29 X
5555 13 28 X
CCCC 14 27 X
7F7F 15 26 X
5H21 16 25 X
OAFA 17 24 X
UPFH 18 23 HPP0
52F8 19 22 2H70
0000 20 21 HC89

Table 8-8. Kernel Troubleshooting Procedure (Continued)

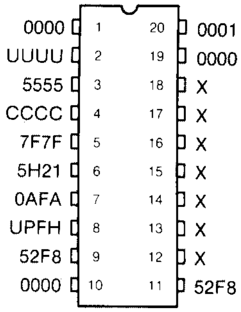
U12


0001 1 14 0001
0001 2 13 X
0001 3 12 X
0001 4 11 X
0001 5 10 X
0000 6 9 0000
0000 7 8 0001

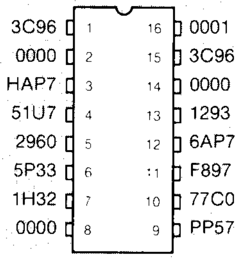
U13


77C0 1 40 0001
0001 2 39 X
0001 3 38 X
0000 4 37 X
0001 5 36 X
X 6 35 X
0000 7 34 X
0001 8 33 X
0001 9 32 X
0001 10 31 X
X 11 30 X
X 12 29 X
5555 13 28 X
X 14 27 X
X 15 26 X
5H21 16 25 X
0AFA 17 24 X
UPFH 18 23 HPP0
52F8 19 22 2H70
0000 20 21 HC89

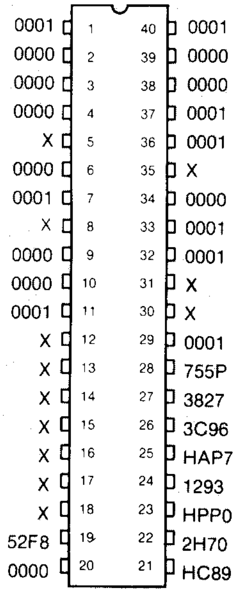
U14


0000 1 20 0001
UUUU 2 19 0000
5555 3 18 X
CCCC 4 17 X
7F7F 5 16 X
5H21 6 15 X
0AFA 7 14 X
UPFH 8 13 X
52F8 9 12 X
0000 10 11 52F8

U15


3C96 1 16 0001
0000 2 15 3C96
HAP7 3 14 0000
51U7 4 13 1293
2960 5 12 6AP7
5P33 6 11 F897
1H32 7 10 77C0
0000 8 9 PP57

U16


0001 1 40 0001
0000 2 39 0000
0000 3 38 0000
0000 4 37 0001
X 5 36 0001
0000 6 35 X
0001 7 34 0000
X 8 33 0001
0000 9 32 0001
0000 10 31 X
0001 11 30 X
X 12 29 0001
X 13 28 755P
X 14 27 3827
X 15 26 3C96
X 16 25 HAP7
X 17 24 1293
X 18 23 HPP0
52F8 19 22 2H70
0000 20 21 HC89

8-261. A1 TROUBLESHOOTING

8-262. The A1 Main Assembly contains the Signature Analyzer circuitry, the Frequency and Time Interval Counter, the Digital to Analog Converters, and the Logic selector circuits.

8-263. The following tests verify specific circuits within the A1 assembly. As each test is performed, the operative status of the indicated circuits is determined. Perform the tests in the order given. The A1 troubleshooting tests are:

Troubleshooting Test	Diagnostic Number
Input Voltage Comparators	—
Signature Analyzer Diag NORM	0-6
Signature Analyzer Diag TEST	0-6
Counter Diag	0-7
Time Interval Diag	0-8
DAC Static Output Diags	0-9, 0-A, 0-B, 0-C
DAC Dynamic Ramp Diag	0-D
Vp+ Zero Offset Diag	0-E
Vp- Zero Offset Diag	0-F

Table 8-9. A1 Troubleshooting Procedure

1. Perform the Input Voltage Comparator Test.

Purpose: The Input Voltage Comparator Test provides a method of verifying the operation of the Data Probe, Timing Pod, Input Compensation circuitry and Input Voltage Comparators. These front end circuits are analog configurations, which are beyond the self diagnostic test routines built into the 5005A.

Procedure:

a. Set the 5005A to the kΩ mode. With the 5005A Data Probe, measure the resistance between ground and each Timing Pod input. The GND input should read 0.000; the START/ST-SP, STOP/QUAL, and CLOCK inputs should each read ≈98k .

b. Set up a pulse generator for a 10 KHz TTL squarewave. Connect the output to the Data Probe tip. Remember to connect the probe ground lead. Using an oscilloscope, trace the signal from the Data Probe tip, through A1 U6(A and B), to the ECL to TTL translators. The signal should be easily traceable, in any function mode, with a reasonable TTL squarewave out of the translator.

c. Repeat for START/ST-SP, STOP/QUAL, and CLOCK inputs of the Timing Pod.

Indications:

A test signal should be traceable from any of the instrument inputs through its respective level translator. The signal level changes from TTL to ECL (out of the Input Voltage Comparator), and back to TTL (out of the translator). If the shape of the squarewave appears suspiciously rounded or misshapen, refer to paragraph 5-13, Input Compensation Adjustments. If the signal does not appear out of the translator, check the ECL output of the Voltage Comparator.

2. Perform the Signature Analyzer NORM Diagnostic (Diag 0-6).

Purpose: The Signature Analyzer NORM Diagnostic provides the user with "key signatures", which help quickly verify the signature analyzer circuits. Checking these key signatures first, will insure functionality of the signature analyzer circuitry. If the following signatures are correct, the signature analyzer portion of the circuitry can be assumed to be properly functioning. If any of the key signatures are incorrect, backtrace through the A1 assembly.

Table 8-9. A1 Troubleshooting Procedure (Continued)

Procedure:

a. Set the diagnostic rotary switches on A3 to 0-6 (S1=0 S2=6).

b. Connect the test signature analyzer as follows:

Controls

START	Falling edge
STOP	Rising edge
CLOCK	Rising edge

Timing Pod

START	A3 TP A15
STOP	A3 TP $\overline{\text{A15}}$
CLOCK	A3 TP $\overline{\text{RD}}$
GND	A3 TP GND

c. Connect the 5005A (UUT) as follows:

Timing Pod

START/ST-SP	A3 TP ST
STOP/QUAL	A3 TP SP
CLOCK	A3 TP CLK
(GND)	A3 TP GND
Data Probe	A3 TP DATA

d. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

CAUTION

This test rapidly opens and closes relays on the A1 Main Assembly. Extended running of this test could cause the relays to fail. Run the test only while necessary.

e. Verify that the light within the UUT Data Probe turns off when the probe tip is grounded, and lights brightly when the probe tip is connected to +5 volts. The test signature analyzer should display the signature "HH03" for +5 volts.

f. With the data probe from the test signature analyzer, verify the following Key Signatures:

Assembly	Component	Pin #	Signature
A3 Microprocessor	U4	34	C0H4
A3 Microprocessor	U10	5	APPP
A3 Microprocessor	U4	37	2U48
A3 Microprocessor	U4	35	60HA
A3 Microprocessor	U4	36	85C2
A3 Microprocessor	J1	$\overline{16}$	HH03 (10MHz)

Indications:

If one or more of the key signatures are incorrect, use a half-splitting or back-tracing technique to locate the bad node in the circuit. The A1 assembly signatures for this diagnostic mode are listed on the following pages.

NOTE

A1U6 is an ECL type device. Signatures taken on A1U6 must be done with a test signature analyzer with ECL data threshold capability.

Table 8-9. A1 Troubleshooting Procedure (Continued)

S.A. Setup — Polarities

Clk: ↑
Start: ↓
Stop: ↑

S.A. Setup — UUT Connections

Clk: RD*
Start/Stop: A15
Stop Qual: A15

Vcc **Signature = HH03**

"X" Signature = Don't Care

U2

Signature	Pin	Pin	Signature
7C10	1	16	HH03
CC32	2	15	0000
6H83	3	14	C000
CFF9	4	13	F526
820C	5	12	F526
HC1F	6	11	HH03
43FH	7	10	1825
0000	8	9	HH03

U3

Signature	Pin	Pin	Signature
0000	1	16	HH03
U288	2	15	0000
HH03	3	14	0716
8376	4	13	58C1
60AH	5	12	58C1
0000	6	11	5PFU
9225	7	10	H8U0
0000	8	9	8C13

U5

Signature	Pin	Pin	Signature
0000	1	16	HH03
2F96	2	15	9225
2F96	3	14	06HF
0000	4	13	242H
HH03	5	12	C0H4
3CFH	6	11	9254
P6FP	7	10	P802
0000	8	9	FA82

U6 *

Signature	Pin	Pin	Signature
X	1	24	1595
X	2	23	1595
X	3	22	X
X	4	21	X
X	5	20	X
X	6	19	X
X	7	18	X
X	8	17	FU6F
X	9	16	X
9604	10	15	X
4115	11	14	X
X	12	13	X

U8

Signature	Pin	Pin	Signature
6945	1	16	HH03
8C13	2	15	A859
242H	3	14	97U4
97U4	4	13	70H9
70H9	5	12	7560
7560	6	11	9254
HH03	7	10	U288
0000	8	9	7F5U

U9

Signature	Pin	Pin	Signature
6945	1	16	HH03
8C13	2	15	7H02
FA82	3	14	0PF1
0PF1	4	13	7286
7286	5	12	06HF
06HF	6	11	16P6
A859	7	10	HH03
0000	8	9	7F5U

U10

Signature	Pin	Pin	Signature
P6C8	1	16	HH03
0000	2	15	1PC8
6945	3	14	8CUP
HH03	4	13	P6C8
2U48	5	12	0000
U24C	6	11	PH06
F526	7	10	1PC8
0000	8	9	6945

U11

Signature	Pin	Pin	Signature
0000	1	16	0000
0000	2	15	0000
0000	3	14	0000
1595	4	13	4115
126U	5	12	9604
0000	6	11	0000
0000	7	10	0000
0000	8	9	HH03

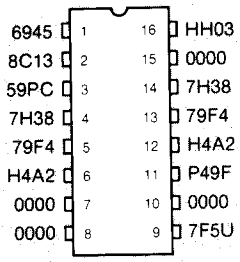
U12

Signature	Pin	Pin	Signature
0000	1	16	0000
0000	2	15	0000
0000	3	14	0000
126U	4	13	FU6F
F896	5	12	1595
0000	6	11	0000
0000	7	10	0000
0000	8	9	HH03

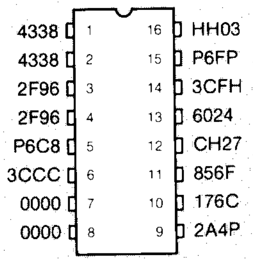
*Set data thresholds on test equipment to ECL logic levels.

Table 8-9. A1 Troubleshooting Procedure (Continued)

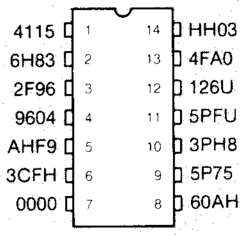
U15


6945 1 16 HH03
8C13 2 15 0000
59PC 3 14 7H38
7H38 4 13 79F4
79F4 5 12 H4A2
H4A2 6 11 P49F
0000 7 10 0000
0000 8 9 7F5U

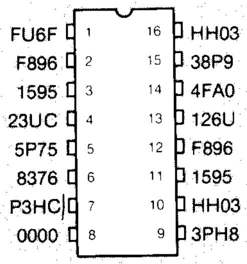
U16


4338 1 16 HH03
4338 2 15 P6FP
2F96 3 14 3CFH
2F96 4 13 6024
P6C8 5 12 CH27
3CCC 6 11 856F
0000 7 10 176C
0000 8 9 2A4P

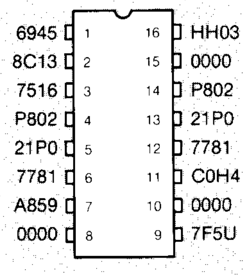
U17


4115 1 14 HH03
6H83 2 13 4FA0
2F96 3 12 126U
9604 4 11 5PFU
AHF9 5 10 3PH8
3CFH 6 9 5P75
0000 7 8 60AH

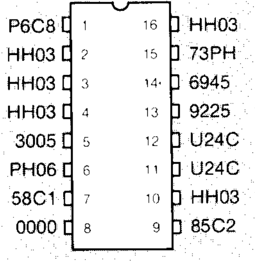
U18


FU6F 1 16 HH03
F896 2 15 38P9
1595 3 14 4FA0
23UC 4 13 126U
5P75 5 12 F896
8376 6 11 1595
P3HC 7 10 HH03
0000 8 9 3PH8

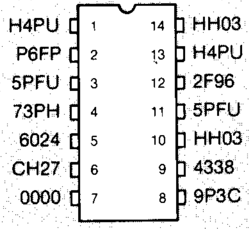
U19


6945 1 16 HH03
8C13 2 15 0000
7516 3 14 P802
P802 4 13 21P0
21P0 5 12 7781
7781 6 11 C0H4
A859 7 10 0000
0000 8 9 7F5U

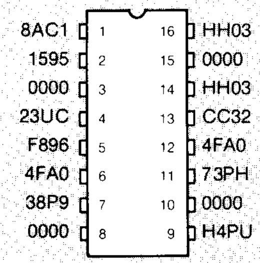
U20


P6C8 1 16 HH03
HH03 2 15 73PH
HH03 3 14 6945
HH03 4 13 9225
3005 5 12 U24C
PH06 6 11 U24C
58C1 7 10 HH03
0000 8 9 85C2

U21


H4PU 1 14 HH03
P6FP 2 13 H4PU
5PFU 3 12 2F96
73PH 4 11 5PFU
6024 5 10 HH03
CH27 6 9 4338
0000 7 8 9P3C

U22


8AC1 1 16 HH03
1595 2 15 0000
0000 3 14 HH03
23UC 4 13 CC32
F896 5 12 4FA0
4FA0 6 11 73PH
38P9 7 10 0000
0000 8 9 H4PU

U26

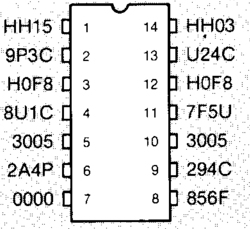

HH15 1 14 HH03
9P3C 2 13 U24C
H0F8 3 12 H0F8
8U1C 4 11 7F5U
3005 5 10 3005
2A4P 6 9 294C
0000 7 8 856F

Table 8-9. A1 Troubleshooting Procedure (Continued)

3. Perform the Signature Analyzer TEST Diagnostic (Diag 0-6).

Purpose: The Signature Analyzer TEST Diagnostic uses the S.A. Test switches on the A3 assembly to tie selected data lines either high (to +5 volts) or low (to ground). These conditions, along with the diagnostic mode, force the FSR into a closed loop which generates stable signatures.

Procedure:

a. Set the diagnostic rotary switches on A3 to 0-6 (S1=0 S2=6).

b. Connect the test signature analyzer as follows:

Controls

START	Falling edge
STOP	Rising edge
CLOCK	Rising edge

Timing Pod

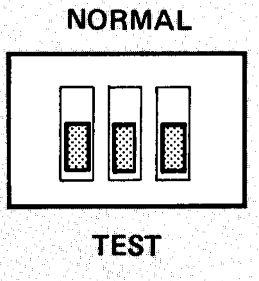
START	A3 TP A15
STOP	A3 TP A15
CLOCK	A3 TP $\overline{RD}$
GND	A3 TP GND

c. Connect the 5005A (UUT) as follows:

Timing Pod

START/ST-SP	A3 TP ST
STOP/QUAL	A3 TP SP
CLOCK	A3 TP CLK
(GND)	A3 TP GND
Data Probe	A3 TP DATA

d. Set all three sections of S.A. Test switch A1 S1 to the TEST position.



e. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

CAUTION

This test rapidly opens and closes relays on the A1 Main Assembly. Extended running of this test could cause the relays to fail. Run the test only while necessary.

Table 8-9. *A1 Troubleshooting Procedure (Continued)*

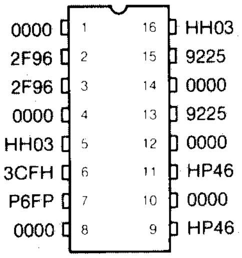
f. Verify the signatures on the individual inputs and outputs of the Feedback Shift Register, as shown below:

S.A. Setup — Polarities	**S.A. Setup — UUT Connections**
Clk: ↑	**Clk:** $\overline{RD}$
Start: ↓	**Start/Stop:** A15
Stop: ↑	**Stop Qual:** A15

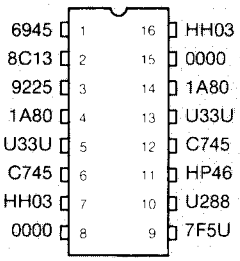
Vcc **Signature** = **HH03**

"X" Signature = **Don't Care**

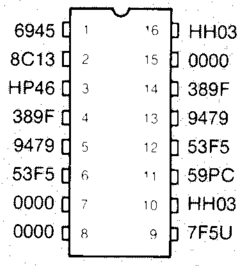
U5


0000 1
2F96 2
2F96 3
0000 4
HH03 5
3CFH 6
P6FP 7
0000 8
16 HH03
15 9225
14 0000
13 9225
12 0000
11 HP46
10 0000
9 HP46

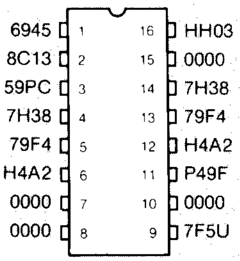
U8


6945 1
8C13 2
9225 3
1A80 4
U33U 5
C745 6
HH03 7
0000 8
16 HH03
15 0000
14 1A80
13 U33U
12 C745
11 HP46
10 U288
9 7F5U

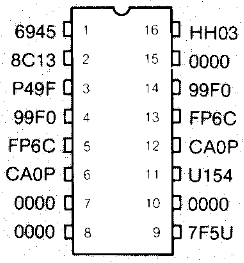
U9


6945 1
8C13 2
HP46 3
389F 4
9479 5
53F5 6
0000 7
0000 8
16 HH03
15 0000
14 389F
13 9479
12 53F5
11 59PC
10 HH03
9 7F5U

U15


6945 1
8C13 2
59PC 3
7H38 4
79F4 5
H4A2 6
0000 7
0000 8
16 HH03
15 0000
14 7H38
13 79F4
12 H4A2
11 P49F
10 0000
9 7F5U

U19


6945 1
8C13 2
P49F 3
99F0 4
FP6C 5
CA0P 6
0000 7
0000 8
16 HH03
15 0000
14 99F0
13 FP6C
12 CA0P
11 U154
10 0000
9 7F5U

Indications:

This closed loop allows the verification of each input and output of the four registers which comprise the Feedback Shift Register. An incorrect signature indicates a faultly device or problem with the printed circuit trace.

NOTE

Be sure to return the Test Switches to their normal positions after testing.

Table 8-9. A1 Troubleshooting Procedure (Continued)

4. Perform the Counter Diagnostic (Diag 0-7).

Purpose: The counter diagnostic exercises nodes on U5, U8, U9, U15, and U19 on the A1 Mainboard, which are not exercised by the signature analyzer diagnostic. The test is initiated as follows:

Procedure:

a. Set the diagnostic rotary switches on A3 to 0-7 (S1=0 S2=7).

b. Connect the test signature analyzer as follows:

Controls

START	Falling edge
STOP	Rising edge
CLOCK	Rising edge

Timing Pod

START	A3 TP A15
STOP	A3 TP A15
CLOCK	A3 TP $\overline{RD}$
GND	A3 TP GND

c. Connect the 5005A (UUT) as follows:

Timing Pod

START/ST-SP	A3 TP ST
STOP/QUAL	A3 TP SP
CLOCK	A3 TP RD CLK
GND	A3 TP GND
Data Probe	A3 TP DATA

d. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

CAUTION

This test rapidly opens and closes relays on the A1 Main Assembly. Extended running of this test could cause the relays to fail. Run the test only while necessary.

e. Place the test signature analyzer data probe on a +5 volt TP within the UUT and verify:

+5 volts	1299

f. The key signature for this diagnostic is on U19 pin 11 (on the A1 Mainboard). This signature should be "911P".

NOTE

This test takes several seconds for each pass.

Table 8-9. A1 Troubleshooting Procedure (Continued)

Indications:

If the key signature is incorrect, use the schematic diagram and the following signatures to determine which of the counter integrated circuits is faulty.

S.A. Setup — Polarities

Clk: ↑
Start: ↓
Stop: ↑

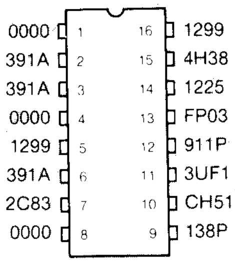
S.A. Setup — UUT Connections

Clk: $\overline{\text{RD}}$
Start/Stop: A15
Stop Qual: A15

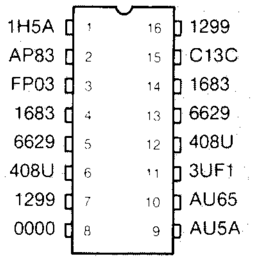
Vcc **Signature** = **1299**

"X" Signature = **Don't Care**

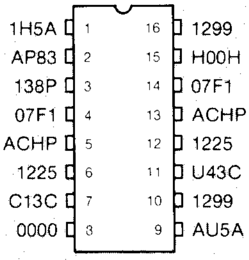
U5


0000 1
391A 2
391A 3
0000 4
1299 5
391A 6
2C83 7
0000 8
1299 16
4H38 15
1225 14
FP03 13
911P 12
3UF1 11
CH51 10
138P 9

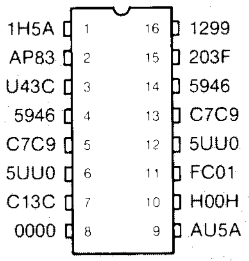
U8


1H5A 1
AP83 2
FP03 3
1683 4
6629 5
408U 6
1299 7
0000 8
1299 16
C13C 15
1683 14
6629 13
408U 12
3UF1 11
AU65 10
AU5A 9

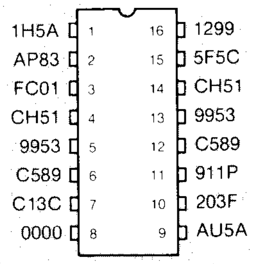
U9


1H5A 1
AP83 2
138P 3
07F1 4
ACHP 5
1225 6
C13C 7
0000 8
1299 16
H00H 15
07F1 14
ACHP 13
1225 12
U43C 11
1299 10
AU5A 9

U15


1H5A 1
AP83 2
U43C 3
5946 4
C7C9 5
5UU0 6
C13C 7
0000 8
1299 16
203F 15
5946 14
C7C9 13
5UU0 12
FC01 11
H00H 10
AU5A 9

U19


1H5A 1
AP83 2
FC01 3
CH51 4
9953 5
C589 6
C13C 7
0000 8
1299 16
5F5C 15
CH51 14
9953 13
C589 12
911P 11
203F 10
AU5A 9

5. Perform the Time Interval Diagnostic (Diag 0-8).

Purpose: The Time Interval Diagnostic is similar to the Counter test, in that it places the four FSR counter ICs in a closed loop for testing. In this mode, however, data selector A1U3 is configured to direct the 10 MHz internal clock into the counter chain, while supplying an arbitrary gate. This test verifies the counter ICs and A1U3 in the T.I. mode of operation.

Procedure:

a. Set the diagnostic rotary switches on A3 to 0-8 (S1=0 S2=8).

b. Connect the test signature analyzer as follows:

Controls

START .... Falling edge
STOP .... Rising edge
CLOCK .... Rising edge

Timing Pod

START .... A3 TP A15
STOP .... A3 TP A15
CLOCK .... A3 TP $\overline{\text{RD}}$
GND .... A3 TP GND

Table 8-9. A1 Troubleshooting Procedure (Continued)

c. Connect the 5005A (UUT) as follows:

Timing Pod

START/ST-SP	A3 TP ST
STOP/QUAL	A3 TP SP
CLOCK	A3 TP CLK
(GND)	A3 TP GND
Data Probe	A3 TP DATA

d. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

e. Observe the display of the UUT. It should show a display of "1.854X", flashing at a rapid rate.

Indications:

If the display appears as described above, the test is passed. Proceed to the next diagnostic. If not, check A1 U3 (pin 3) for a 10 MHz TTL squarewave. If the squarewave is present, check A1 U3 for the following signatures:

S.A. Setup — Polarities

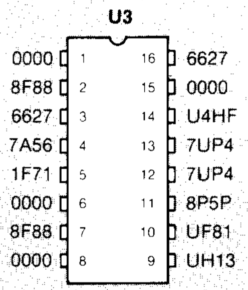
Clk: ↑
Start: ↓
Stop: ↑

S.A. Setup — UUT Connections

Clk: $\overline{RD}$
Start/Stop: A15
Stop Qual: A15

Vcc **Signature = 6627**

"X" Signature = Don't Care



6. Perform the DAC Static Output Diagnostics (Diags 0-9 through 0-C).

Purpose: The four diagnostics, which make up the DAC static output test, instruct the microprocessor to program preselected dc voltages into all four DACs, U1, U4, U7, and U13 on the A1 assembly. The voltages can be measured on TP's 1, 2, 3, and 4 on A1, and should be within ±1% of the programmed value. The four diagnostics shift the programmed voltages to each of the four DACs, as indicated in the table below.

Procedure:

a. Sequentially set the diagnostic rotary switches on A3 to each of the four positions listed below. For each position, measure the dc voltage at TPs 1, 2, 3, and 4. Remember to turn the UUT LINE switch from ON to OFF then back to ON again, each time a new diagnostic is selected.

A3 S1	A3 S2	A1 U1 (A1 TP1)	A1 U4 (A1 TP2)	A1 U7 (A1 TP3)	A1 U13 (A1 TP4)
0	9	0.0V	+7.65V	0.45V	-7.65V
0	A	-7.65V	0.0V	+7.65V	0.45V
0	B	0.45V	-7.65V	0.0V	+7.65V
0	C	+7.65V	0.45V	-7.65V	0.0V

Table 8-9. A1 Troubleshooting Procedure (Continued)

Indications:

This test gives a static indication of the programmability and accuracy of each of the four DACs. The inputs of all four DACs are configured in parallel. Address decoder U2A enables each DAC. If any of the DAC voltages are incorrect, check the Current-to-Voltage translators U14, A – D, and the indicated DAC output.

7. Perform the DAC Dynamic Ramp Diagnostic (Diag 0-D).

Purpose: The DAC Dynamic Ramp diagnostic instructs the microprocessor to program all four DACs to output a ramp waveform. The ramp cycles from +7.65 volts to -7.65 volts. By observing the output of each DAC, the accuracy and linearity can be monitored.

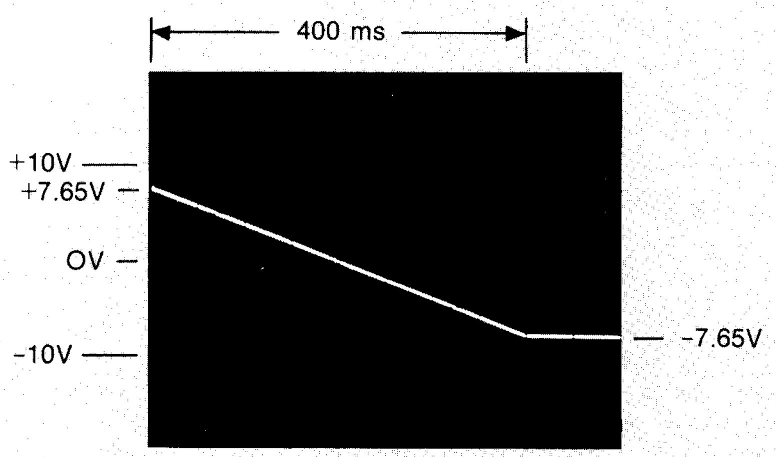
Procedure:

a. Set the diagnostic rotary switches on A3 to 0-D (S1=0 S2=D).

b. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

c. Connect an oscilloscope to each of the four DAC test points in turn, and observe the ramp outputs. The outputs from the DACs can be obtained as a voltage waveform at the following test points:

A1U1=TP1 A1U4=TP2 A1U7=TP3 A1U13=TP4



Scope:

Volts/Div 5V (10:1)
Time/Div .... 50 ms
Coupling .... DC
Auto/Norm .... (NORM)

This waveform can be viewed by setting up an oscilloscope as follows:

Timebase .... 50 ms/div
Trigger .... + slope
Vertical gain .... 2 V/div

Table 8-10. A2 Troubleshooting Procedure (Continued)

Indications:

By setting the voltage sensitivity, vertical position, and horizontal position controls, the different areas of the waveform can be viewed. This allows checks for missing levels and nonlinearitys.

Note that the smallest increment on the stairstep waveform should be 30mv in height. The 0 volt level is displayed twice i.e. lasts twice as long as the other levels.

8. Perform the VP- Zero Offset Value Diagnostic (Diag 0-E).

Purpose: The VP+ Test finds the offset value necessary to zero the VP- circuits. The microprocessor first programs A1K2 Data Switch Relay to the calibration position. The microprocessor programs DAC A1 U1 to a starting voltage level and checks the DATA (PROBE) line from the Mainboard to establish if a transition on the input comparators has occurred. If not the microprocessor increments the program value to the DAC, until a transition occurs. This value is established to be the zero offset value for the comparators and DACs. This value is sent to the display.

Procedure:

a. Set the diagnostic rotary switches on A3 to 0-E (S1=0 S2=E).

b. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

CAUTION

This test rapidly opens and closes relays on the A1 Main assembly. Extended running of this test could cause the relays to fail. Run the test only while necessary.

c. The display should contain a reading between -0.10 and 0.10.

Indications:

If a zero offset between -0.10 and +0.10 volts is not obtained, the display will usually contain a +12.50 or -12.50 result. This indicates that the diagnostic program did not recognize a transition, and continued stepping to its programmable limits. If this happens, try the procedure again. If it is still bad, monitor the output of A1U12 for a transition while repeating the diagnostic. Follow the transition through the A1 circuitry to DATA (PROBE) J1 pin $\overline{28}$.

9. Perform the VP- Zero Offset Value Diagnostic (Diag 0-F).

Purpose: The VP- Test finds the offset value necessary to zero the VP- circuits. The microprocessor first programs A1K2 Data Switch Relay to the calibration position. The microprocessor programs DAC U1 to a starting voltage level and checks the DATA (PROBE) line from the Mainboard to establish if a transition on the input comparators has occurred. If not the microprocessor increments the program value to the DAC, until a transition occurs. This value is established to be the zero offset value for the comparators and DACs. This value is sent to the display.

Procedure:

a. Set the diagnostic rotary switches on A3 to 0-F (S1=0 S2=F).

b. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

CAUTION

This test rapidly opens and closes relays on the A1 Main Assembly. Extended running of this test could cause the relays to fail. Run the test only while necessary.

c. The display should contain a reading between -0.10 and 0.10.

Indications:

If a zero offset between -0.10 and +0.10 volts is not obtained, the display will usually contain a +12.50 or -12.50 result. This indicates that the diagnostic program did not recognize a transition, and continued stepping to its programmable limits. If this happens, try the procedure again. If it is still bad, monitor the output of A1U12 for a transition while repeating the diagnostic. Follow the transition through the A1 circuitry to DATA (PROBE) J1 pin $\overline{28}$.

8-264. A2 DVM TROUBLESHOOTING

CAUTION

The DVM board is sensitive to fingerprints and other contamination. Do not handle board with bare fingers except at the edges. Contamination can cause malfunctions in the DVM circuitry.

8-265. The following tests verify specific circuits within the A2 assembly. As each test is performed, the operative status of the indicated circuits is determined. Perform the tests in the order given. Read the complete test description before initiating any DVM diagnostics. The A2 troubleshooting tests are:

Troubleshooting Test	Diagnostic Number
Test Point Measurements	—
Zero Offset Value / 25V range	1-0
Zero Offset Value / 250V range	1-3
Auto-Calibration / 25V range	1-1
Auto-Calibration / 250 V range	1-4
Uncorrected Reading / 25 V range	1-2
Uncorrected Reading / 250 V range	1-5
Zero Offset Value / Ohms Mode	1-6
Reference Voltage / Ohms Mode	1-7
Measured Voltage / Ohms Mode	1-8
Overvoltage Detector Test	—

8-266. Prior to troubleshooting the A2 DVM assembly, it is recommended that the technician read and understand the DVM theory of operation given in this section.

Table 8-10. A2 Troubleshooting Procedure

1. Perform the Test Point Measurements.

Purpose: The following two tests provide preliminary verification that the DVM reference voltage (+10.00V) and the assembly sub-clock signals are present.

Procedure:

a. Connect a dc voltmeter to the A2 assembly as follows: positive (red) lead to TP1, and negative (black) to TP2. The dc voltage should be 10.000 volts, ± 1 mV. If the voltage is only slightly off, attempt to adjust using A2 R2.

b. With a frequency counter, measure the frequency of the TTL sub-clock signal at A2 U7 pin 8. This is the 10 MHz main clock, divided by a factor of "61". The output frequency should be ≈ 163.93 kHz. If the frequency is incorrect, check the 10 MHz main clock input at U8 pin 2, and the output of U8 pin 15 for 655.73 kHz.

Indications:

If a fault is located at these areas, using the schematic locate the problem and correct before checking for further faults.

Table 8-10. A2 Troubleshooting Procedure (Continued)

2. Zero Offset Value for 25 Volt Range (Diag 1–0).

Purpose: The purpose of the Zero Offset Value diagnostic is to instruct the microprocessor to force the DVM assembly into the 25 V range, and ground the input. The resultant voltage measurement represents the offset voltage at zero volts for the 25 V range. The diagnostic activates the range and grounds the input through the Analog Crosspoint Switch. The measured offset is displayed during the test.

Procedure:

a. Set the diagnostic rotary switches on A3 to 1–0 (S1=1 S2=0).

b. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

c. Verify that the 5005A displays a zero offset value between –0020. and +0020.

Indications:

If the display contains an incorrect result, check the status of A2U2 pin 9 (it should be ground). Check the status of Q3 and Q4 (Q3 should be on, Q4 should be off). Check the Data/Cal relay (it should be energized).

3. Zero Offset Value for 250 Volt Range (Diag 1-0).

Purpose: The purpose of the Zero Offset Value diagnostic is to instruct the microprocessor to force the DVM assembly into the 250 V range, and ground the input. The resultant voltage measurement represents the offset voltage at zero volts for the 250 V range. The diagnostic activates the range and grounds the input through the Analog Crosspoint Switch. The measured offset is displayed during the test.

Procedure:

a. Set the diagnostic rotary switches on A3 to 1–3 (S1=1 S2=3).

b. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

c. Verify that the 5005A displays a zero offset value between –0020. and +0020.

Indications:

If the display contains an incorrect result, check the status of A2U2 pin 9 (it should be ground). Check the status of Q3 and Q4 (Q3 should be on, Q4 should be off). Check the Data/Cal relay (it should be energized).

4. AUTO-CAL for 25 Volt Range (Diag 1-1).

Purpose: The purpose of the Auto-Cal diagnostic is to instruct the microprocessor to force the DVM assembly into the 25V range, and connect the input to the 10.00 volt precision reference. The resultant voltage measurement represents the DVM voltage value with a known input voltage (+10.00). The diagnostic activates the range and connects the input through the Analog Crosspoint Switch. The measured value is displayed during the test.

Procedure:

a. Set the diagnostic rotary switches on A3 to 1-1 (S1=1 S2=1).

b. Turn the UUT LINE switch from ON to OFF then back back to ON. This initiates the diagnostic.

c. Verify that the 5005A displays a Auto-Cal value between 09500. and 10100.

Indications:

If the display contains an incorrect result, check the status of A2U2 pin 9 (it should be -10.00V). Check the status of Q3 and Q4 (Q4 should be on, Q3 should be off). Check the Data/Cal relay (it should be energized).

5. AUTO-CAL For 250 Volt Range (Diag 1-4).

Purpose: The purpose of the Auto-Cal diagnostic is to instruct the microprocessor to force the DVM assembly into the 250 V range, and connect the input to the +10.00 volt precision reference. The resultant voltage measurement represents the DVM voltage value with a known input voltage (+10.00). The diagnostic activates the range and connects the input through the Analog Crosspoint Switch. The measured value is displayed during the test.

Table 8-10. A2 Troubleshooting Procedure (Continued)

Procedure:

a. Set the diagnostic rotary switches on A3 to 1-4 (S1=1 S2=4).

b. Turn the UUT LINE switch from ON to OFF then back back to ON. This initiates the diagnostic.

c. Verify that the 5005A displays a Auto-Cal value between 00940. and 01020.

Indications:

If the display contains an incorrect result, check the status of A2U2 pin 9 (it should be +10.00V). Check the status of Q3 and Q4 (Q3 should be on, Q4 should be off). Check the Data/Cal relay (it should be energized).

6. Uncorrected Reading For The 25 Volt Range (Diag 1-2).

Purpose: The purpose of the uncorrected reading diagnostic is to instruct the microprocessor to force the DVM assembly into the 25 V range, and connect the input to the Data Probe path. The resultant voltage measurement represents the DVM voltage value through the Data Probe path. The diagnostic activates the range and connects the input through the Analog Crosspoint Switch. The measured value is displayed during the test.

The microprocessor enables the voltage probe path and measurements of the probe tip voltage are continuously made. This raw voltage measurement is sent to the microprocessor. No arithmetic is performed. The raw measurement value is sent to the display. This is a test of the probe capability to measure a raw voltage properly. Note that the displayed voltage will not be the actual voltage present at the tip due to offsets and scaling. The formula for computing the actual voltage at the probe tip is:

$$\text{Voltage at Tip} = \frac{\text{Uncorrected reading - Zero offset}}{\text{10.00 volt ref reading - Zero offset}} \quad \text{X10V}$$

Procedure:

a. Set the diagnostic rotary switches on A3 to 1-2 (S1=1 S2=2).

b. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

c. Verify that the 5005A displays a uncorrected DVM value within the allowable tolerance, as defined above.

Indications:

If the display contains an incorrect result, check the status of A2K2 (it should not be energized). Check the status of Q3 and Q4 (Q4 should be on, Q3 should be off).

7. Uncorrected Reading For The 250 Volt Range (Diag 1-5).

Purpose: The purpose of the uncorrected reading diagnostic is to instruct the microprocessor to force the DVM assembly into the 250 V range, and connect the input to the Data Probe path. The resultant voltage measurement represents the DVM voltage value through the Data Probe path. The diagnostic activates the range and connects the input through the Analog Crosspoint Switch. The measured value is displayed during the test.

The microprocessor enables the voltage probe path and measurements of the probe tip voltage are continuosly made. This raw voltage measurement is sent to the microprocessor. No arithmetic is performed. The raw measurement value is sent to the display. This is a test of the probe capability to measure a raw voltage properly. Note that the displayed voltage will not be the actual voltage present at the tip due to offsets and scaling. The formula for computing the actual voltage at the probe tip is:

$$\text{Voltage at Tip} = \frac{\text{Uncorrected reading - Zero offset}}{\text{10.00 volt ref reading - Zero offset}} \quad \text{X10V}$$

Procedure:

a. Set the diagnostic rotary switches on A3 to 1-5 (S1=1 S2=5).

b. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

c. Verify that the 5005A displays a uncorrected DVM value within the allowable tolerance, as defined above.

Table 8-10. A2 Troubleshooting Procedure (Continued)

Indications:

If the display contains an incorrect result, check the status of A2K2 (it should not be energized). Check the status of Q3 and Q4 (Q3 should be on, Q4 should be off).

8. Zero Offset Value For Ohms (Diag 1-6).

Purpose: The purpose of the Zero Offset Value diagnostic is to instruct the microprocessor to force the DVM assembly into the 2.5 V range (Ohms only), and ground the input. The resultant voltage measurement represents the offset voltage at zero volts for the Ohms mode. The diagnostic activates the range and grounds the input through the Analog Crosspoint Switch. The measured offset is displayed during the test.

Procedure:

a. Set the diagnostic rotary switches on A3 to 1-6 (S1=1 S2=6).

b. Turn the UUT LINE switch from ON to OFF then back back to ON. This initiates the diagnostic.

c. Verify that the 5005A displays a zero offset value between -0020. and +0020.

Indications:

If the display contains an incorrect result, check the status of A2U2 pin 9 (it should be ground). Check the status of Q3 and Q4 (Q4 should be off, Q3 should be off). Check the Data/Cal relay (it should be energized).

9. Reference Voltage For Ohms (Diag 1-7).

Purpose: The purpose of the reference voltage diagnostic is to instruct the microprocessor to force the DVM assembly into the 2.5 V range (Ohms only), and connect the input to the +2.0 volt Reference. The resultant voltage measurement represents the DVM -2.0 volt reference value for the Ohms mode. The diagnostic activates the range and connects the input through the Analog Crosspoint Switch. The measured value is displayed during the test.

Procedure:

a. Set the diagnostic rotary switches on A3 to 1-7 (S1=1 S2=7).

b. Turn the UUT LINE switch from ON to OFF then back back to ON. This initiates the diagnostic.

c. Verify that the 5005A displays an Ohms reference value between 19500 and 20500.

If the display contains an incorrect result, check the status of A2U2 pin 9 (it should be +2.00 volts). Check the status of Q3 and Q4 (Q4 should be off, Q3 should be off). Check the status of A2K2 (it should be energized).

10. Measure Voltage for Ohms (Diag 1-8).

Purpose: The purpose of the measure voltage diagnostic is to instruct the microprocessor to force the DVM assembly into the 2.5 V range (Ohms mode), connect the DVM input to the Data Probe path, and connect the +2.0 volt current source, through K1, to the Data Probe reference resistor. The resultant voltage measurement represents the DVM reference voltage value through the Data Probe path. The diagnostic activates the range and connects the input through the Analog Crosspoint Switch. The measured value is displayed during the test.

The microprocessor enables the voltage probe path and measurements through the probe reference resistance are continuously made. This raw voltage measurement is sent to the microprocessor. No arithmetic is performed. The raw measurement value is sent to the display. This is a test of the probe capability to measure a raw voltage properly. Note that the displayed voltage will not be the actual voltage present at the tip due to offsets and scaling.

Procedure:

a. Set the diagnostic rotary switches on A3 to 1-8 (S1=1 S2=8).

b. Turn the UUT LINE switch from ON to OFF then back back to ON. This initiates the diagnostic.

c. Verify that the 5005A displays a OHms reference value between -0020. and +0020.

Indications:

If the display contains an incorrect result, check the status of A2K2 and K1 (both should be energized). Check the status of Q3 and Q4 (Q4 should be off, Q3 should be off). Follow the +2.00 volts from A2U3 pin 6, through K1, through the A5 Data Probe, back to the A2 DVM assembly A2K2, to the input of the A/D U4 pin 15.

Table 8-10. A2 Troubleshooting Procedure (Continued)

11. Perform the Overvoltage Detector test.

Purpose: The Overvoltage Detector circuit, consisting of U6, Q5, and assorted support circuitry, is normally a passive or non-active circuit. The purpose of the circuit is to detect an overvoltage condition at A2 R19. This point is normally 2.0 volts, generated by U3 for use during the Ohmmeter mode. If, during the Ohmmeter mode, the Data Probe tip is placed on a dc voltage, the Overvoltage Detector should sense the error and force the interrupt line OVOL low. This halts the microprocessor and the measurement, and opens the OHM Control relay, protecting the A2 DVM assembly.

Procedure:

a. To test the Overvoltage Detector circuit, place the 5005A into the OHMs (k) mode.

b. Monitor OVOL, by connecting an oscilloscope or logic probe to the collector of A2 Q5.

c. First, force an overvoltage condition by momentarily connecting the output of U3 pin 6 to +5 volts. The (lower) U6 Op-amp should switch states, turning Q5 on, which causes OVOL to go low.

d. Next, force an undervoltage condition, by momentarily connecting the output of U3 pin 6 to ground. The (upper) U6 Op-amp should switch states, turning Q5 on, which causes OVOL to go low.

Indications:

When either an overvoltage or undervoltage condition exists at U3 pin 6, the Overvoltage Detector should respond by driving OVOL low. Overvoltage is any dc level greater than 2.95 volts, undervoltage is any dc level less than 0.9 volts. With the overvoltage condition removed, the circuit should return to its quiescent state with OVOL high.

8-267. A3 TROUBLESHOOTING

8-268. The A3 Microprocessor Assembly contains the microprocessor, RAM, ROM, and I/O devices. A majority of the A3 circuitry is verified by the Kernel Troubleshooting Procedure in *Table 8-8*. The following diagnostics verify the Output Port and the Timer circuits.

Troubleshooting Test	Diagnostic Number
Output Port Diagnostic	0-4
Timer Diagnostic	0-5

Table 8-11. A3 Troubleshooting Procedure

1. Perform the Output Port Diagnostic (Diag 0-4).

a. Set the diagnostic rotary switches on A3 to 0-4 (S1=0 S2=4).

b. Connect the test signature analyzer as follows:

Controls

START	Falling edge
STOP	Rising edge
CLOCK	Rising edge

Timing Pod

START	A3 TP A15
STOP	A3 TP A15
CLOCK	A3 TP $\overline{RD}$
GND	A3 TP GND

A2 DVM ASSEMBLY TROUBLESHOOTING
A3 MICROPROCESSOR ASSEMBLY

Table 8-11. A3 Troubleshooting Procedure (Continued)

Note

The display cable can be disconnected for convenience.

c. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

d. Verify the signatures for the four memory devices, U4, U8, U11, and U13 and buffers U7 and U10 as listed below:

S.A. Setup — Polarities

Clk: ↑
Start: ↓
Stop: ↑

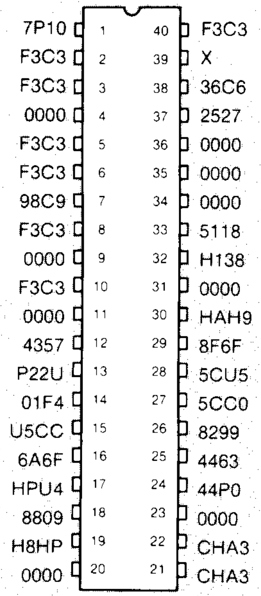
S.A. Setup — UUT Connections

Clk: $\overline{RD}$
Start/Stop: A15
Stop Qual: A15

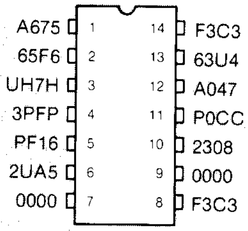
Vcc **Signature = F3C3**

"X" Signature = Don't Care

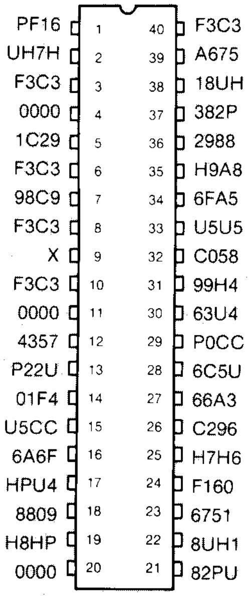
U4


7P10 1 40 F3C3
F3C3 2 39 X
F3C3 3 38 36C6
0000 4 37 2527
F3C3 5 36 0000
F3C3 6 35 0000
98C9 7 34 0000
F3C3 8 33 5118
0000 9 32 H138
F3C3 10 31 0000
0000 11 30 HAH9
4357 12 29 8F6F
P22U 13 28 5CU5
01F4 14 27 5CC0
U5CC 15 26 8299
6A6F 16 25 4463
HPU4 17 24 44P0
8809 18 23 0000
H8HP 19 22 CHA3
0000 20 21 CHA3

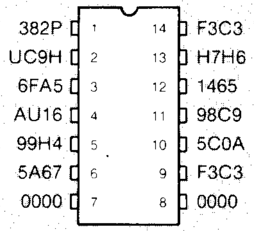
U7


A675 1 14 F3C3
65F6 2 13 63U4
UH7H 3 12 A047
3PFP 4 11 P0CC
PF16 5 10 2308
2UA5 6 9 0000
0000 7 8 F3C3

U8


PF16 1 40 F3C3
UH7H 2 39 A675
F3C3 3 38 18UH
0000 4 37 382P
1C29 5 36 2988
F3C3 6 35 H9A8
98C9 7 34 6FA5
F3C3 8 33 U5U5
X 9 32 C058
F3C3 10 31 99H4
0000 11 30 63U4
4357 12 29 P0CC
P22U 13 28 6C5U
01F4 14 27 66A3
U5CC 15 26 C296
6A6F 16 25 H7H6
HPU4 17 24 F160
8809 18 23 6751
H8HP 19 22 8UH1
0000 20 21 82PU

U10


382P 1 14 F3C3
UC9H 2 13 H7H6
6FA5 3 12 1465
AU16 4 11 98C9
99H4 5 10 5C0A
5A67 6 9 F3C3
0000 7 8 0000

U11

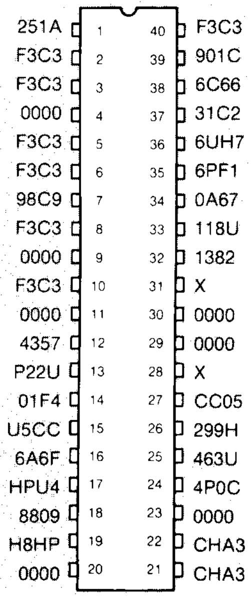

251A 1 40 F3C3
F3C3 2 39 901C
F3C3 3 38 6C66
0000 4 37 31C2
F3C3 5 36 6UH7
F3C3 6 35 6PF1
98C9 7 34 0A67
F3C3 8 33 118U
0000 9 32 1382
F3C3 10 31 X
0000 11 30 0000
4357 12 29 0000
P22U 13 28 X
01F4 14 27 CC05
U5CC 15 26 299H
6A6F 16 25 463U
HPU4 17 24 4P0C
8809 18 23 0000
H8HP 19 22 CHA3
0000 20 21 CHA3

Table 8-11. A3 Troubleshooting Procedure (Continued)

Indications:

This test individually checks out each of the four memory devices and their buffers. A bad signature on any memory or buffer (output) indicates a bad device.

2. Perform the Timer Diagnostic (Diag 0-5).

Purpose: The purpose of the timer diagnostic is to verify proper operation of the A3 Timer circuits.

Procedure:

a. Set the diagnostic rotary switches on A3 to 0-5 (S1=0 S2=045).

b. Connect the test signature analyzer as follows:

Controls

START	Falling edge
STOP	Rising edge
CLOCK	Rising edge

Timing Pod

START	A3 TP A15
STOP	A3 TP A15
CLOCK	A3 TP $\overline{\text{RD}}$
GND	A3 TP GND

c. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.
d. Verify the key signatures as follows:

Location	Key Signature
A3 U16 pin 7	F8P6
A3 U16 pin 21	0352
A3 U16 pin 3	0000 (flashing)
A3 U16 pin 2	0000

Indications:

The timer circuitry utilizes the divided down input 10 Mhz clock (2.6 MHz) and internal down-counters within U8 to generate the one-second gate interval reset to the microprocessor. If any of the signatures are incorrect, backtrace the circuit.

8-269. A4 TROUBLESHOOTING

8-270. The A4 Keyboard and Display Assembly contains the instrument display LEDs, status LEDs, and keyboard. The following diagnostics verify all LEDs and the keyboard.

Troubleshooting Test	Diagnostic Number
Display Test (Part I)	1-9
Display Test (Part II)	1-A
Keyboard Test	1-B

Table 8-12. A4 Troubleshooting Procedure

1. Perform Part I of the Display Test (Diag 1-9).

Purpose: The purpose of Part I of the display test is to light all the front panel LEDs, allowing a visual confirmation of all front panel indicators.

Procedure:

a. Set the diagnostic rotary switches on A3 to 1-9 (S1=1 S2=9).

b. Insure that the display ribbon cable is connected to the A3 Microprocessor Assembly.

c. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

d. Verify that all front panel LEDs, except GATE and UNSTABLE light continuously. LEDs GATE and UNSTABLE should flash at approximately a five hertz rate. The MSD in the display should have only the center segment lighted.

Indications:

If any of the LEDs fail to light, refer to the disassembly procedures, remove the A4 assembly and replace the LED.

2. Perform Part II of the display test (Diag 1-A).

Purpose: Part II of the display test marches all the possible display characters across the display, in a repeating routine. Additionally, the diagnostic provides signatures for the A3 Display Driver IC.

Procedure:

a. Set the diagnostic rotary switches on A3 to 1-A (S1=1 S2=A).

b. Connect the test signature analyzer as follows:

Controls

START	Falling edge
STOP	Rising edge
CLOCK	Rising edge

Timing Pod

START	A3 TP A15
STOP	A3 TP $\overline{\text{A15}}$
CLOCK	A3 TP $\overline{\text{WR}}$
GND	A3 TP GND

c. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

d. Observe the display and verify that the characters listed below scroll from right to left across the rightmost five display digits.

0.1.2.3.4.5.6.7.8.9.A.C.F.H.P.U.----

All other remaining LEDs on the front panel should not be lighted. The diagnostic takes approximately eleven seconds to complete one cycle.

Table 8-12. A4 Troubleshooting Procedure (Continued)

e. Verify the signatures listed below, by probing the Display Decoder Driver IC, A3 U6.

S.A. Setup — Polarities

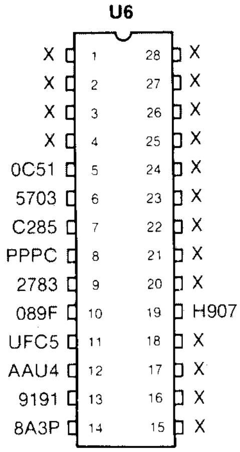
Clk: ↑
Start: ↓
Stop: ↑

S.A. Setup — UUT Connections

Clk: $\overline{\text{RD}}$
Start/Stop: A15
Stop Qual: A15

Vcc **Signature** = **H907**

"X" Signature = **Don't Care**


U6
1 X
2 X
3 X
4 X
5 0C51
6 5703
7 C285
8 PPPC
9 2783
10 089F
11 UFC5
12 AAU4
13 9191
14 8A3P
15 X
16 X
17 X
18 X
19 H907
20 X
21 X
22 X
23 X
24 X
25 X
26 X
27 X
28 X

Indications:

If the character pattern is incorrect, or one or more of the signatures on A3U6 are incorrect, suspect A3U6.

3. Perform the Keyboard Test (Diag 1-B).

Purpose: The Keyboard test configures the instrument to respond to a keypress by the operator by displaying the corresponding front panel key number.

Procedure:

a. Set the diagnostic rotary switches on A3 to 1-B (S1=1 S2=B).

b. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

c. In any sequence, press each of the front panel keys, and verify the display responds with key codes as listed below.

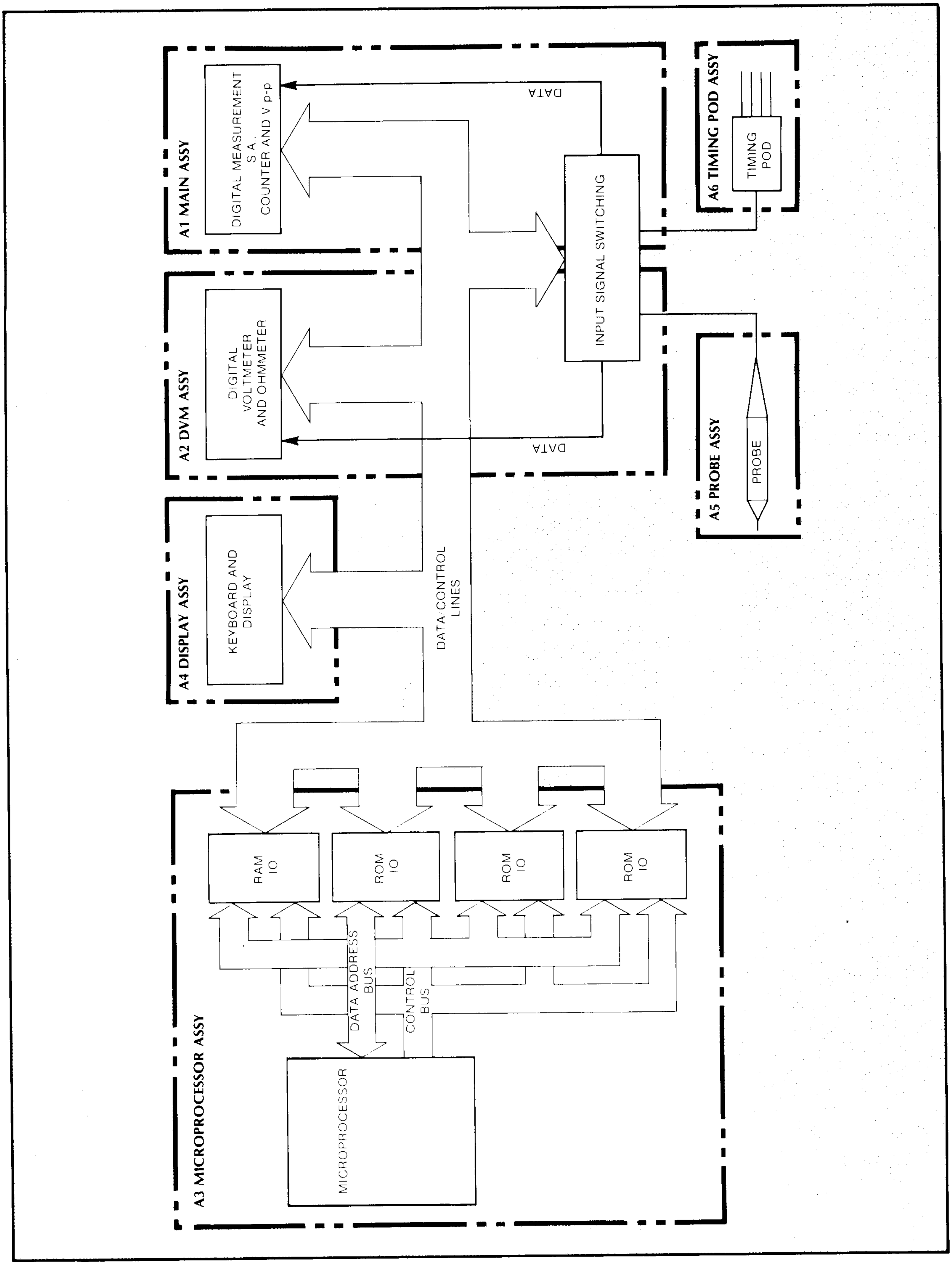
KEY	DISPLAY
NORM ○	1 6
QUAL ●	1 7
kHz ●	0 5
TOTLZ ●	1 3
ms ●	0 9
kΩ ●	0 1

Table 8-12. A4 Troubleshooting Procedure (Continued)

KEY	DISPLAY
DCV ⊡	0 4
V ⊡	1 2
Vp+ ⊡	0 8
Vp ⊡	0 0
DATA ☐	0 2
CLOCK ☐	1 4
ST-TP-QL ☐	1 0
⇧	1 8
⇩	1 6
CLOCK ☐	0 3
START ☐	1 5
STOP ☐	1 1
QUAL ☐	0 7

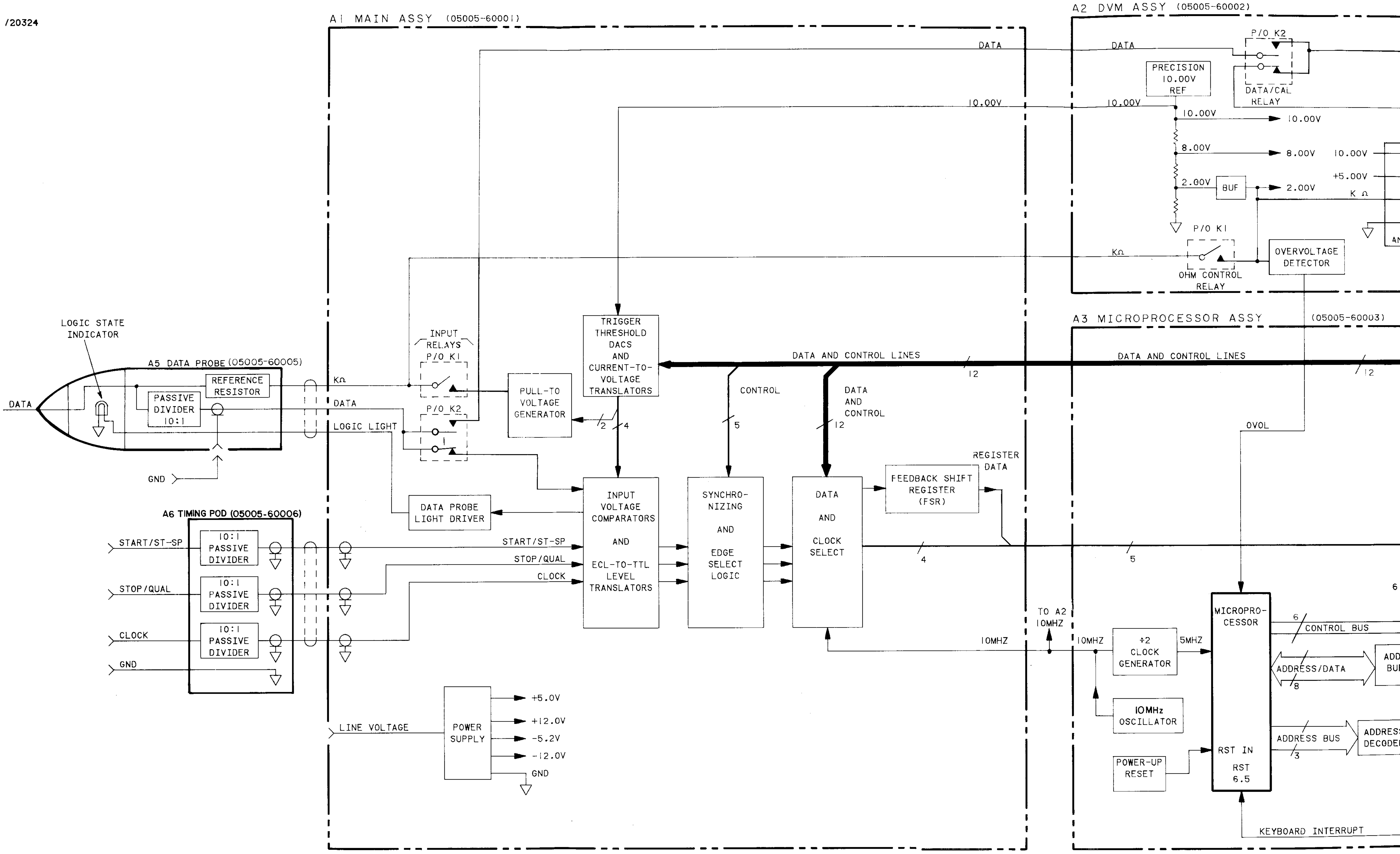
Indications:

If any one of the key responses are incorrect, suspect the corresponding pushbutton key. If several key responses are incorrect, check for a shorted or open trace or bad ribbon cable wire in the X and Y matrix lines from A3 U3. If all the key responses are incorrect, suspect A3 U3.


A1 MAIN ASSY
DIGITAL MEASUREMENT S.A. COUNTER AND V p-p
DATA
INPUT SIGNAL SWITCHING
A6 TIMING POD ASSY
TIMING POD
A2 DVM ASSY
DIGITAL VOLTMETER AND OHMMETER
DATA
A5 PROBE ASSY
PROBE
A4 DISPLAY ASSY
KEYBOARD AND DISPLAY
DATA CONTROL LINES
A3 MICROPROCESSOR ASSY
RAM IO
ROM IO
ROM IO
ROM IO
DATA ADDRESS BUS
CONTROL BUS
MICROPROCESSOR

5005A SIMPLIFIED BLOCK DIAGRAM

/20324


A1 MAIN ASSY (05005-60001)
A2 DVM ASSY (05005-60002)
A3 MICROPROCESSOR ASSY (05005-60003)
A5 DATA PROBE (05005-60005)
A6 TIMING POD (05005-60006)
LOGIC STATE INDICATOR
DATA
REFERENCE RESISTOR
PASSIVE DIVIDER 10:1
GND
KΩ
DATA
LOGIC LIGHT
INPUT RELAYS P/O K1
P/O K2
PULL-TO VOLTAGE GENERATOR
TRIGGER THRESHOLD DACS AND CURRENT-TO-VOLTAGE TRANSLATORS
DATA AND CONTROL LINES
12
CONTROL
5
DATA AND CONTROL
12
2
4
DATA PROBE LIGHT DRIVER
INPUT VOLTAGE COMPARATORS AND ECL-TO-TTL LEVEL TRANSLATORS
SYNCHRO-NIZING AND EDGE SELECT LOGIC
DATA AND CLOCK SELECT
FEEDBACK SHIFT REGISTER (FSR)
REGISTER DATA
4
5
START/ST-SP
STOP/QUAL
CLOCK
GND
10:1 PASSIVE DIVIDER
10:1 PASSIVE DIVIDER
10:1 PASSIVE DIVIDER
START/ST-SP
STOP/QUAL
CLOCK
10MHZ
TO A2 10MHZ
LINE VOLTAGE
POWER SUPPLY
+5.0V
+12.0V
-5.2V
-12.0V
GND
DATA
P/O K2
DATA/CAL RELAY
PRECISION 10.00V REF
10.00V
10.00V
10.00V
10.00V
8.00V
8.00V
2.00V
BUF
2.00V
10.00V
+5.00V
K Ω
P/O K1
KΩ
OHM CONTROL RELAY
OVERVOLTAGE DETECTOR
DATA AND CONTROL LINES
12
OVOL
6
MICROPRO-CESSOR
6
CONTROL BUS
10MHZ
÷2 CLOCK GENERATOR
5MHZ
ADDRESS/DATA
8
10MHz OSCILLATOR
ADDRESS BUS
3
POWER-UP RESET
RST IN
RST 6.5
KEYBOARD INTERRUPT

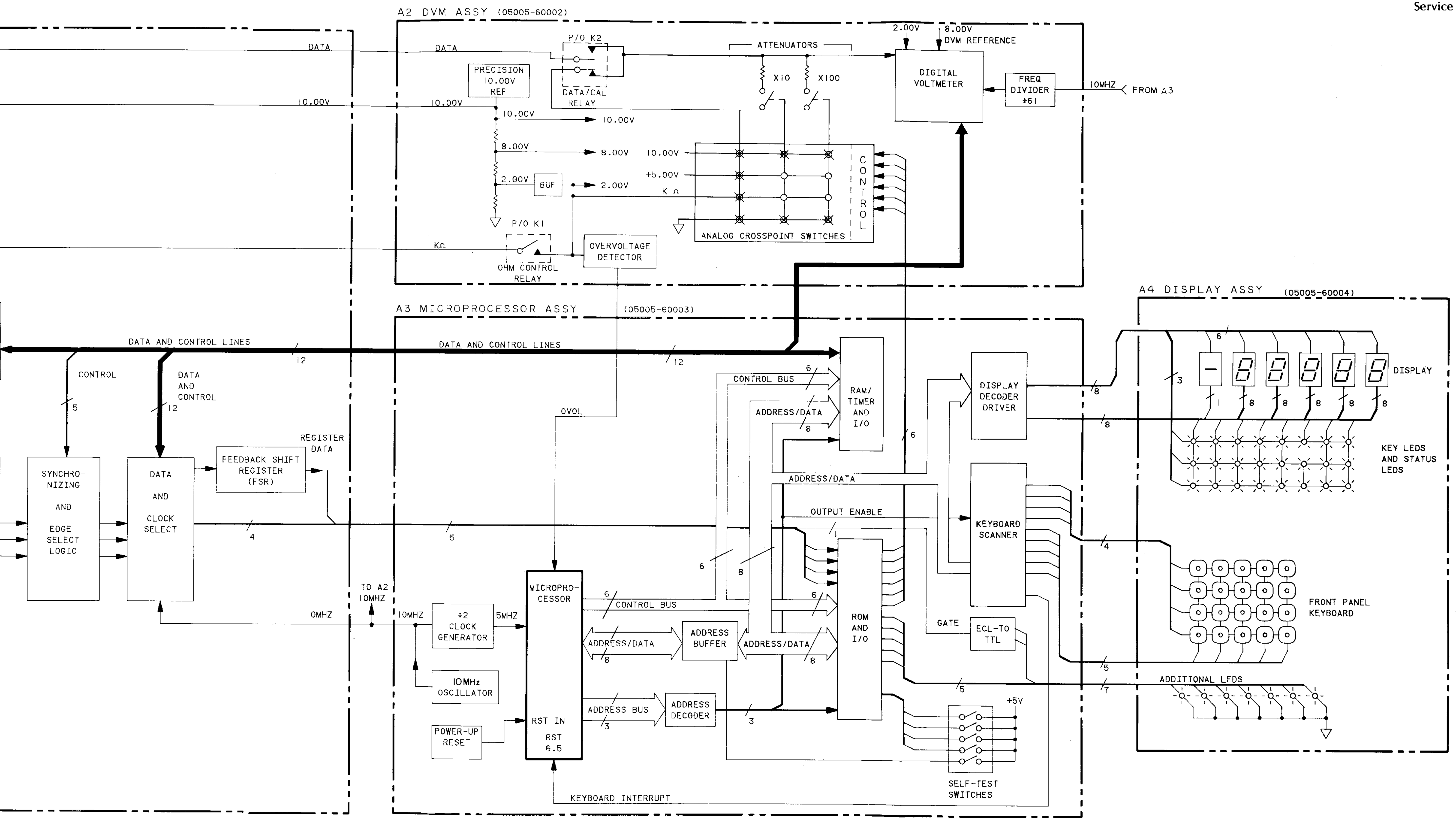
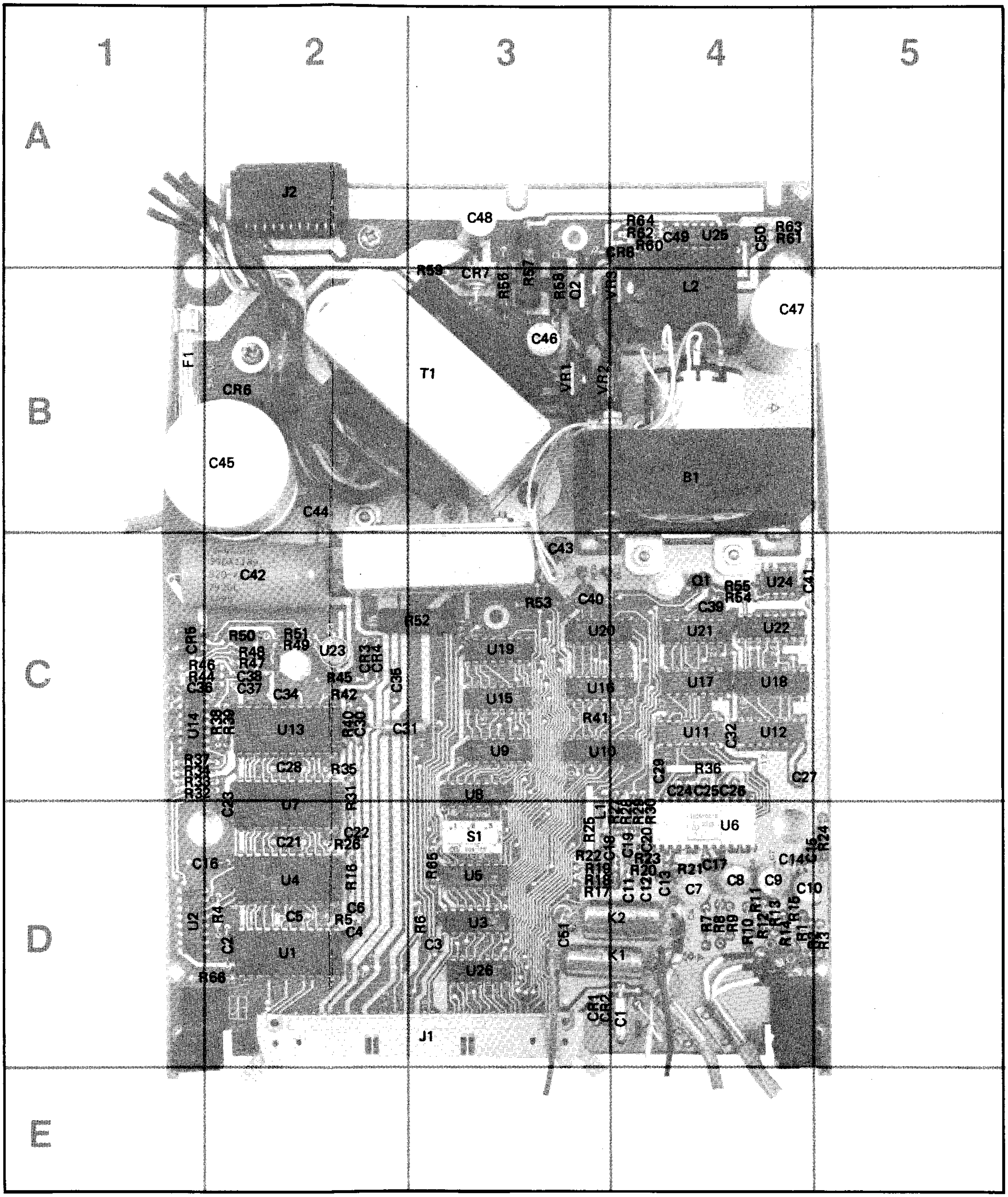

A2 DVM ASSY (05005-60002)
DATA
DATA
P/O K2
DATA/CAL RELAY
PRECISION 10.00V REF
10.00V
10.00V
10.00V
10.00V
8.00V
8.00V
2.00V
BUF
2.00V
P/O K1
OHM CONTROL RELAY
KΩ
OVERVOLTAGE DETECTOR
ATTENUATORS
X10
X100
10.00V
+5.00V
K Ω
ANALOG CROSSPOINT SWITCHES
CONTROL
2.00V
8.00V DVM REFERENCE
DIGITAL VOLTMETER
FREQ DIVIDER ÷61
10MHZ
FROM A3
A3 MICROPROCESSOR ASSY (05005-60003)
DATA AND CONTROL LINES
12
DATA AND CONTROL LINES
12
CONTROL
5
DATA AND CONTROL
12
REGISTER DATA
FEEDBACK SHIFT REGISTER (FSR)
SYNCHRO-NIZING AND EDGE SELECT LOGIC
DATA AND CLOCK SELECT
4
5
OVOL
TO A2 10MHZ
10MHZ
10MHZ
÷2 CLOCK GENERATOR
5MHZ
10MHz OSCILLATOR
POWER-UP RESET
MICROPRO-CESSOR
RST IN
RST 6.5
6
CONTROL BUS
ADDRESS/DATA
8
ADDRESS BUFFER
ADDRESS/DATA
8
ADDRESS BUS
3
ADDRESS DECODER
3
6
8
CONTROL BUS
6
ADDRESS/DATA
8
RAM/ TIMER AND I/O
6
ADDRESS/DATA
OUTPUT ENABLE
1
6
ROM AND I/O
5
SELF-TEST SWITCHES
+5V
KEYBOARD INTERRUPT
DISPLAY DECODER DRIVER
KEYBOARD SCANNER
GATE
ECL-TO TTL
A4 DISPLAY ASSY (05005-60004)
6
3
8
8
1
8
8
8
8
8
DISPLAY
KEY LEDS AND STATUS LEDS
4
FRONT PANEL KEYBOARD
5
7
ADDITIONAL LEDS

Figure 8-20. Block Diagram


1
2
3
4
5
A
B
C
D
E
J2
C48
R64
R62
R60
C49
U25
C50
R63
R61
R59
CR7
R56
R57
R58
Q2
VR3
CR8
L2
C47
C46
F1
CR6
T1
VR1
VR2
C45
B1
C44
C43
C42
Q1
R55
R54
U24
C41
R53
C40
C39
R52
R50
R51
R49
CR5
R48
R47
U23
CR3
CR4
U19
U20
U21
U22
R46
R44
C36
C38
C37
R45
C35
C34
R42
U15
U16
U17
U18
U14
R38
R39
U13
R40
C30
C31
R41
U11
C32
U12
U9
U10
R37
R34
R33
R32
C28
R35
C29
R36
C27
C33
U7
R31
U8
L1
C24
C25
C26
U6
C21
C22
R26
S1
R25
R24
C16
U4
R18
R65
U5
R22
R19
R17
C18
C19
C20
R23
R20
R21
C17
C14
C15
C11
C12
C13
C7
C8
C9
C10
U2
R4
C5
C6
R5
C4
R6
U3
C51
K2
R7
R8
R9
R10
R11
R12
R13
R14
R15
R1
R2
R3
C2
U1
C3
K1
R66
U26
CR1
CR2
C1
J1

Part of Figure 8-21. A1 Main Assembly Schematic Diagram

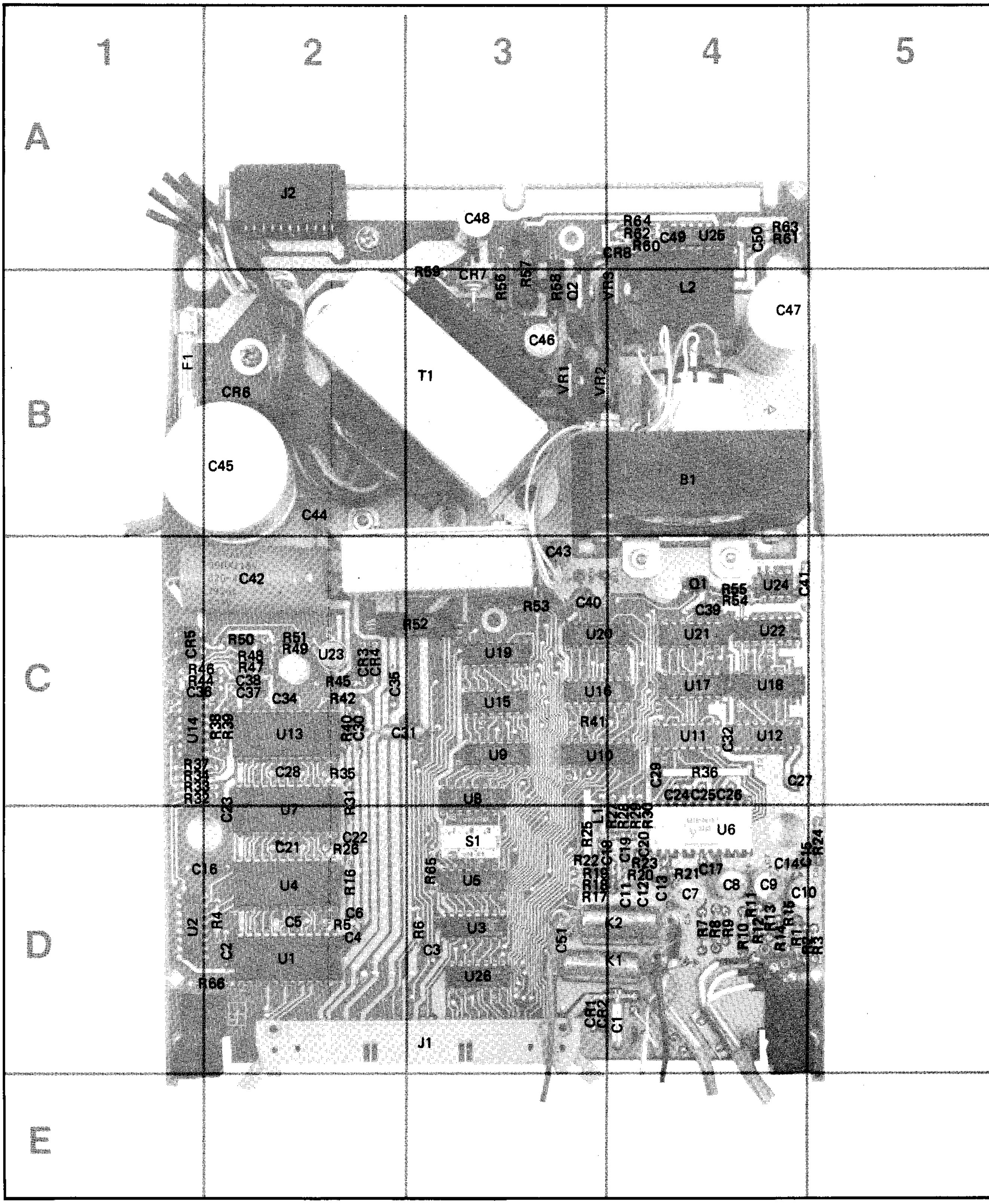
Figure 8-20
BLOCK DIAGRAM

(See Page 8-95)

GRID LOCATIONS

REF DESIG	C/L	SCHEMATIC
A1C1	D-4	C-1
A1C2	D-2	D-5
A1C3	D-3	C-9
A1C4	D-2	D-5
A1C5	D-2	D-5
A1C6	D-2	D-4
A1C7	D-4	D-1
A1C8	D-4	D-1
A1C9	D-4	E-1
A1C10	D-5	E-1
A1C11	D-4	C-6
A1C12	D-4	C-6
A1C13	D-4	E-2
A1C14	D-5	B-6
A1C15	D-5	D-2
A1C16	D-2	C-4
A1C17	D-4	E-2
A1C18	D-4	D-2
A1C19	D-4	D-6
A1C20	D-4	E-2
A1C21	D-2	C-4
A1C22	D-2	C-5
A1C23	D-2	C-5
A1C24	D-4	D-2
A1C25	D-4	D-2
A1C26	D-4	D-2
A1C27	C-5	B-5
A1C28	C-2	C-5
A1C29	C-4	E-6
A1C30	C-2	B-4
A1C31	C-3	B-3
A1C32	C-4	E-4
A1C33	N/A	N/A
A1C34	C-2	B-4
A1C35	C-3	A-6
A1C36	C-2	D-5
A1C37	C-2	B-4
A1C38	C-2	D-5
A1C39	C-4	A-6
A1C40	C-4	E-3
A1C41	C-5	E-3
A1C42	C-2	A-4
A1C43	C-3	A-5
A1C44	B-2	A-6
A1C45	B-2	A-4
A1C46	B-3	A-5
A1C47	B-5	A-6
A1C48	A-3	A-4
A1C49	A-4	A-5
A1C50	A-4	A-5
A1C51	D-3	C-2
A1CR1	D-4	C-1
A1CR2	D-4	C-1
A1CR3	C-2	D-6
A1CR4	C-2	D-6
A1CR5	C-2	A-4
A1CR6	B-2	A-4
A1CR7	B-3	A-5
A1CR8	A-4	A-6
A1F1	B-2	A-4
A1K1	D-4	C-1
A1K2	D-4	C-1
A1L1	D-4	D-3
A1L2	B-4	A-5
A1Q1	C-4	E-3
A1Q2	B-3	A-4
A1R1	D-5	E-1
A1R2	D-5	D-1
A1R3	D-5	E-1
A1R4	D-2	D-5
A1R5	D-2	D-5
A1R6	D-3	B-3
A1R7	D-4	D-2
A1R8	D-4	D-1
A1R9	D-4	D-1
A1R10	D-4	D-1
A1R11	D-4	D-1
A1R12	D-4	D-1
A1R13	D-4	E-1
A1R14	D-4	D-1
A1R15	D-5	E-1
A1R16	D-2	C-6
A1R17	D-4	C-6
A1R18	D-4	C-6
A1R19	D-4	C-6
A1R20	D-4	C-6
A1R21	D-4	C-6
A1R22	D-4	C-6
A1R23	D-4	D-6
A1R24	D-5	B-6
A1R25	D-3	B-9, C-9
A1R26	D-2	C-4
A1R27	D-4	D-6
A1R28	D-4	D-6
A1R29	D-4	B-6
A1R30	D-4	B-6
A1R31	D-2	C-5
A1R32	D-2	D-5
A1R33	C-2	D-5
A1R34	C-2	C-5
A1R35	C-2	B-5
A1R36	C-4	D-3
A1R37	C-2	C-5
A1R38	C-2	C-5
A1R39	C-2	C-5
A1R40	C-2	B-4
A1R41	C-4	
A1R42	C-2	B-4
A1R43	N/A	N/A
A1R44	C-2	B-5
A1R45	C-2	D-6
A1R46	C-2	B-5
A1R47	C-2	D-6
A1R48	C-2	C-6
A1R49	C-2	D-6
A1R50	C-2	D-6
A1R51	C-2	D-6
A1R52	C-3	A-6
A1R53	C-3	C-9
A1R54	C-4	E-4
A1R55	C-4	E-5
A1R56	B-3	A-4
A1R57	B-3	A-4
A1R58	B-3	A-6
A1R59	B-3	A-4
A1R60	A-4	A-5
A1R61	A-5	A-5
A1R62	A-4	A-6
A1R63	A-5	A-5
A1R64	A-4	A-6
A1R65	D-3	D-7
A1R66	D-2	C-9
A1S1	D-3	B-6
A1U1	D-2	D-5
A1U2	D-2	B-4, D-8
A1U3	D-3	C-9
A1U4	D-2	C-4
A1U5	D-3	C-6, D-7
A1U6	D-4	D-2
A1U7	D-2	C-5
A1U8	D-3	C-7
A1U9	C-3	C-8
A1U10	C-4	D-8
A1U11	C-4	E-6
A1U12	C-4	E-4
A1U13	C-2	B-4
A1U14	C-2	B-5, C-5, D-5
A1U15	C-3	B-8
A1U16	C-4	D-9
A1U17	C-4	E-7
A1U18	C-4	E-4
A1U19	C-3	B-9
A1U20	C-4	D-7
A1U21	C-4	E-8
A1U22	C-4	E-7, E-5
A1U23	C-2	D-6
A1U24	C-4	E-3
A1U25	A-4	A-5
A1U26	D-3	A-5, E-8, D-9

Part of Figure 8-21. A1 Main Assembly/A7 Line Module Schematic Diagram


1
2
3
4
5
A
B
C
D
E
J2
C48
R64
R62
R60
C49
U25
C50
R63
R61
CR8
R59
CR7
R56
R57
R68
Q2
VR3
L2
C47
C46
F1
CR6
T1
VR1
VR2
C45
B1
C44
C43
C42
Q1
R55
R54
U24
C41
R53
C40
C39
R52
U20
U21
U22
CR5
R50
R51
R49
R48
R47
R46
R44
C36
C38
C37
U23
CR3
CR4
C35
U19
C34
R45
R42
U16
U17
U18
U15
U14
R38
R39
U13
R40
C30
C31
R41
U11
C32
U12
U9
U10
R37
R34
R33
R32
C28
R35
C29
R36
C27
C23
U7
R31
U8
C24
C25
C26
L1
R25
R27
R29
R30
U6
S1
C22
C21
R26
C18
C19
C20
R22
R23
R24
C15
C16
R65
R19
R18
R17
R20
R21
C17
C14
U4
R16
U5
C11
C12
C13
C7
C8
C9
C10
C6
U2
R4
C5
R5
C4
R6
U3
C51
K2
R7
R8
R9
R10
R11
R12
R13
R14
R15
R1
R2
R3
C2
U1
C3
U26
K1
R66
CR1
CR2
C1
J1

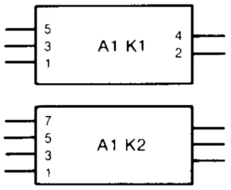
Part of Figure 8-21. A1 Main Assembly Schematic Diagram

Figure 8-2
BLOCK DIAGRAM

(See Page 8-95

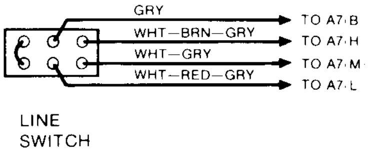
A1J1 CONNECTOR PINOUT
CIRCUIT SIDE OF BOARD

	$\overline{\text{K4}}$	$\overline{30}$	●	■	30	END OF MEASURE	
	$\overline{\text{K3}}$	$\overline{29}$	●	●	29	LSB COUNT	
	DATA (PROBE)	$\overline{28}$	●	●	28	REGISTER DATA	
	GATE	$\overline{27}$	●	●	27	POLARITY DIFF	——TD0
	TD1	$\overline{26}$	●	●	26	SYNC	
——TD2	START EDGE	$\overline{25}$	●	■	25	CLOCK EDGE	——DA0
——$\overline{\text{SIGN}}$	$\overline{\text{COMBINED STOP/START}}$	$\overline{24}$	●	●	24	$\overline{\text{START MEASURE}}$	
——DA1	STOP/QUAL EDGE	$\overline{23}$	●	●	23	POP	
	$\overline{\text{OUTPUT SHIFT ENABLE}}$	$\overline{22}$	●	●	22	SIGNATURE-TI	——TD4
——TD3	DATA STROBE	$\overline{21}$	●	●	21	FREQ-SIGN	——$\overline{\text{POP}}$
——TD5	COUNT	$\overline{20}$	●	■	20	$\overline{\text{DSTR}}$	
	QUAL ENABLE	$\overline{19}$	●	●	19	+5V	——TD7
	+5V	$\overline{18}$	●	●	18	+5V	
	GND	$\overline{17}$	●	●	17	GND	
	10 MHz	$\overline{16}$	●	●	16	GND	
	N.C.	$\overline{15}$	●	■	15	GND	
	N.C.	$\overline{14}$	●	●	14	+10.00V	
	N.C.	$\overline{13}$	●	●	13	N.C.	
	N.C.	$\overline{12}$	●	●	12	N.C.	
	N.C.	$\overline{11}$	●	●	11	N.C.	
	N.C.	$\overline{10}$	●	■	10	N.C.	
	N.C.	$\overline{9}$	●	●	9	+12V	
	N.C.	$\overline{8}$	●	●	8	GND (A)	
	N.C.	$\overline{7}$	●	●	7	-12V	
	N.C.	$\overline{6}$	●	●	6	GND (D)	
	N.C.	$\overline{5}$	●	■	5	+5V	
	N.C.	$\overline{4}$	●	●	4	-5.2V	
	N.C.	$\overline{3}$	●	●	3	N.C.	
	N.C.	$\overline{2}$	●	●	2	N.C.	
	N.C.	$\overline{1}$	●	■	1	N.C.	



A1 RELAYS PINOUT
(TOP VIEW)

W2 (HP PART #05005-60101)

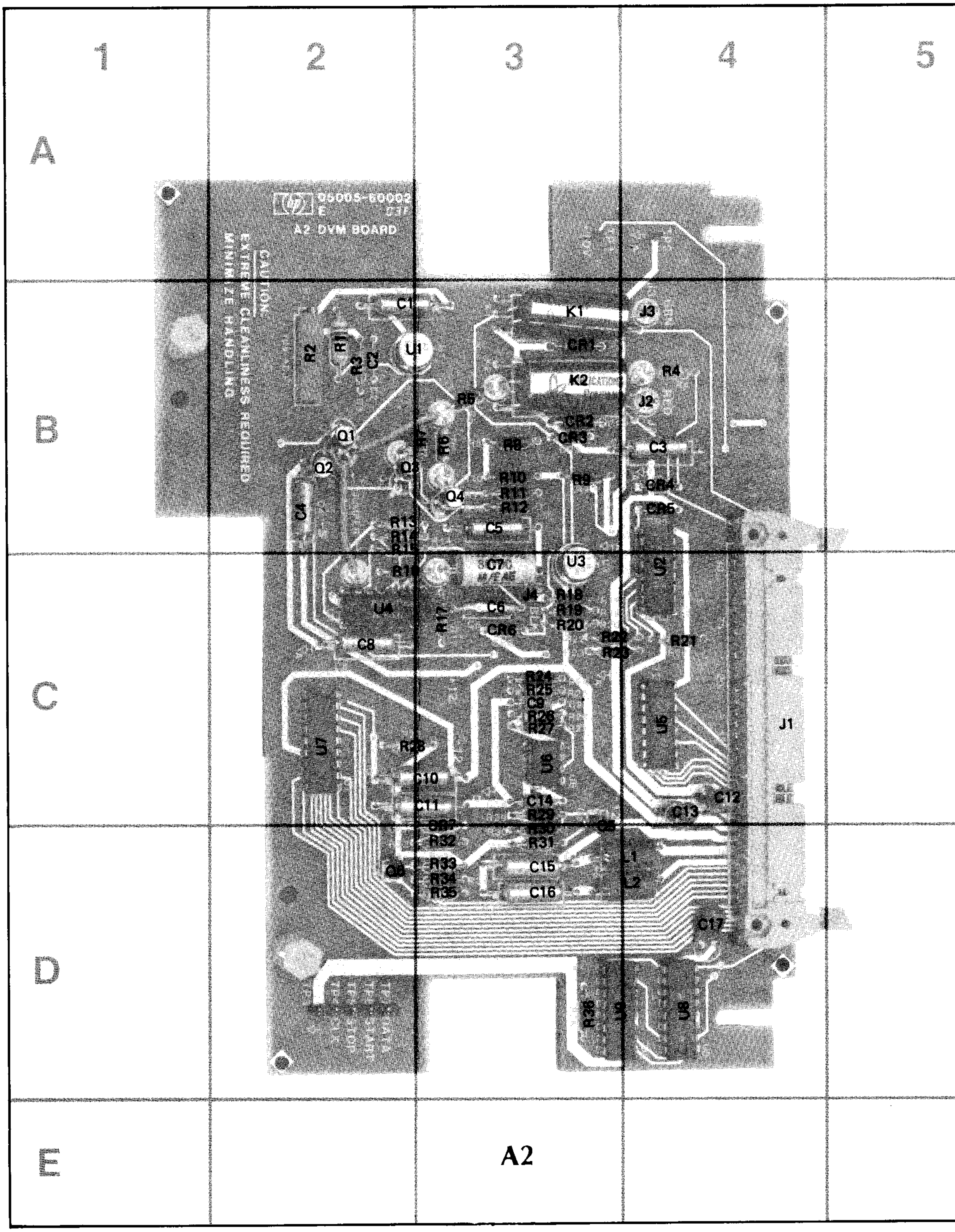


Troubleshooting:

The following troubleshooting procedures are provided to verify the proper operation, and isolate malfunctioning components on the A1 Main Assembly. Procedures begin with paragraph 8-261.

Troubleshooting Test	**Diagnostic Number**
Input Voltage comparators	—
Signature Analyzer Diag NORM	0–6
Signature Analyzer Diag TEST	0–6
Counter Diag	0–7
Time Interval Diag	0–8
DAC Static Output Diags	0–9, 0–A, 0–B, 0–C
DAC Dynamic Ramp Diag	0–D
Vp+ Zero Offset Diag	0–E
Vp– Zero Offset Diag	0–F

Part of Figure 8-21. A1 Main Assembly/A7 Line Module Schematic Diagram

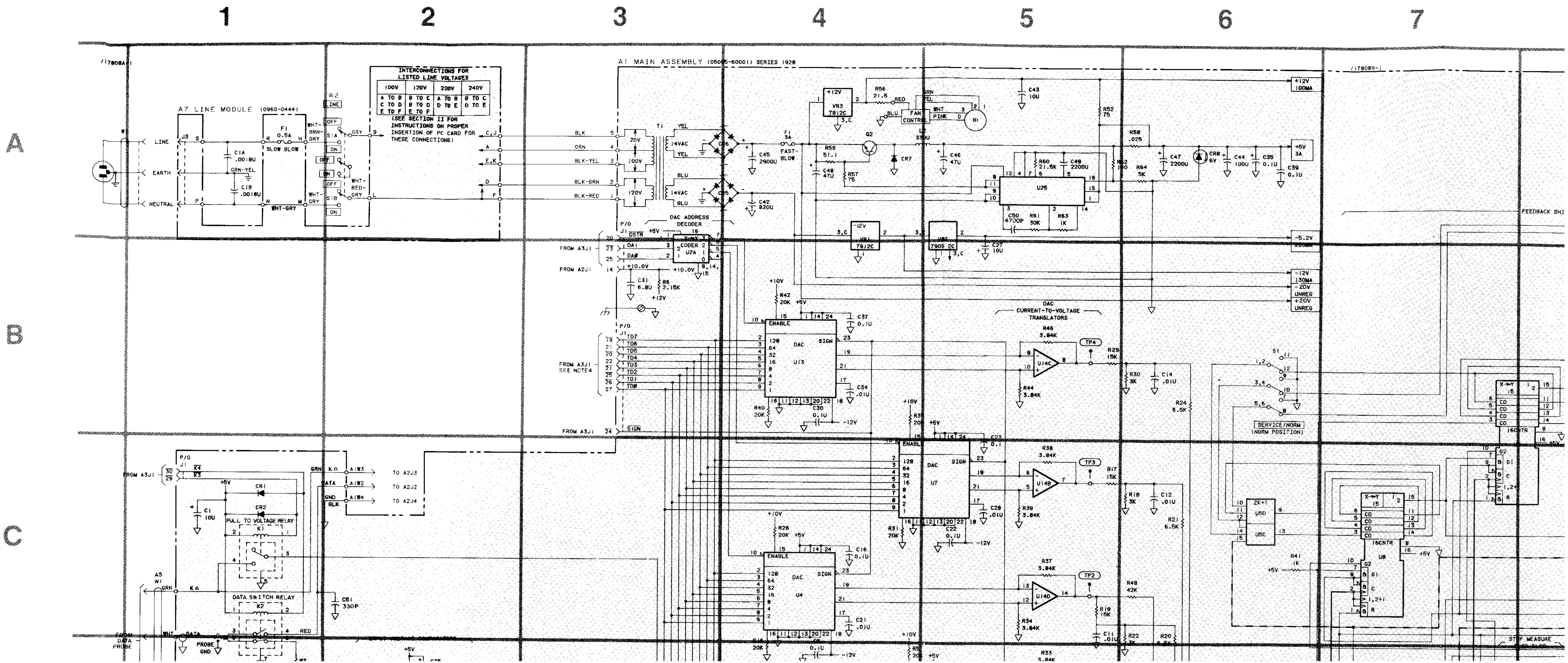


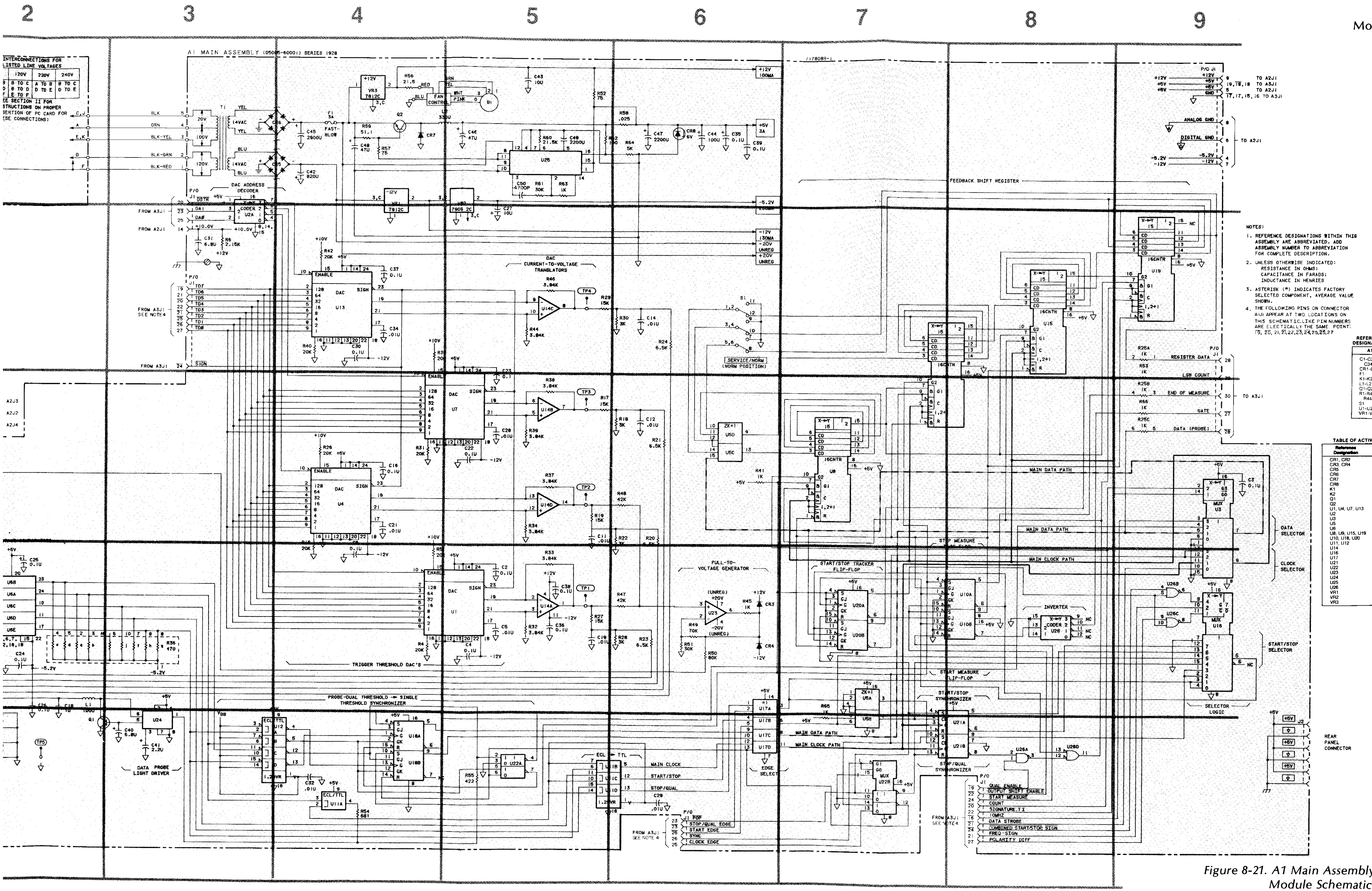
1
2
3
4
5
A
B
C
D
E
05005-60002
A2 DVM BOARD
CAUTION:
EXTREME CLEANLINESS REQUIRED
MINIMIZE HANDLING
C1
R2
R1
R3
C2
U1
K1
J3
CR1
K2
R4
J2
R5
CR2
CR3
Q1
Q2
Q3
R7
R6
R8
C3
R10
R11
R12
R9
CR4
CR5
Q4
C4
R13
R14
R15
C5
R16
C7
U3
U2
U4
J4
R18
R19
R20
C6
R17
CR6
C8
R22
R23
R21
R24
R25
C9
R26
R27
U7
R28
U6
U5
J1
C10
C11
C14
R29
C12
C13
CR7
R32
R30
R31
Q5
Q6
R33
R34
R35
C15
C16
L1
L2
C17
R36
U9
U8
A2

Part of Figure 8-22. A2 DVM Assembly Schematic Diagram

Figu
A1/A7 SCHEMATIC DIA

(See pag


1
2
3
4
5
6
7
A
B
C
A7 LINE MODULE (0960-0444)
LINE
EARTH
NEUTRAL
J3
C1A .0018U
C1B .0018U
GRN-YEL
F1 0.5A SLOW BLOW
WHT-GRY
WHT-BRN-GRY
WHT-RED-GRY
W2
LINE
S1A
S1B
OFF
ON
INTERCONNECTIONS FOR LISTED LINE VOLTAGES
100V
120V
220V
240V
A TO B C TO D E TO F
B TO C D TO E E TO F
A TO B D TO E E TO F
B TO C D TO E
(SEE SECTION II FOR INSTRUCTIONS ON PROPER INSERTION OF PC CARD FOR THESE CONNECTIONS)
A1 MAIN ASSEMBLY (05065-60001) SERIES 1928
BLK
ORN
BLK-YEL
BLK-GRN
BLK-RED
T1
20V
100V
120V
14VAC
YEL
BLU
CR6
CR5
C45 2900U
C42 820U
F1 3A FAST-BLOW
VR3 7812C
+12V
R56 21.5
RED
BLU
FAN CONTROL
GRN
YEL
WHT
PINK
B1
Q2
R59 51.1
C48 47U
R57 75
CR7
L2 330U
C46 47U
C43 10U
R52 75
R58 .025
R62 100
R64 5K
R60 21.5K
C49 2200U
U25
C50 4700P
R61 30K
R63 1K
C47 2200U
CR8 6V
C44 100U
C35 0.1U
C39 0.1U
+12V 100MA
+5V 3A
-5.2V 200MA
-12V 130MA
-20V UNREG
+20V UNREG
VR1 7812C
VR2 7905 2C
C27 10U
-12V
FEEDBACK SHI
DAC ADDRESS DECODER
CODER U2A
DSTR
DA1
DA0
FROM A3J1
FROM A2J1
+10.0V
C31 6.8U
R6 2.15K
+12V
P/O J1
TD7
TD6
TD5
TD4
TD3
TD2
TD1
TD0
FROM A3J1 SEE NOTE4
SIGN
R42 20K
+10V
+5V
ENABLE
DAC
U13
U7
U4
C37 0.1U
C34 .01U
R40 20K
C30 0.1U
C23 0.1
C20 .01U
C22 0.1U
C16 0.1U
C21 .01U
R26 20K
R31 20K
DAC CURRENT-TO-VOLTAGE TRANSLATORS
R46 3.84K
U14C
TP4
R29 15K
R30 3K
C14 .01U
R44 3.84K
R24 6.5K
R38 3.84K
U14B
TP3
R17 15K
R18 3K
C12 .01U
R39 3.84K
R21 6.5K
R37 3.84K
U14D
TP2
R48 42K
R19 15K
R34 3.84K
C11 .01U
R22
R20
R33 3.84K
S1
SERVICE/NORM (NORM POSITION)
U5D
U5C
2K+1
R41 1K
X→Y
16CNTR
U8
CD
G1
G2
1,2+1
STEP MEASURE
FROM A3J1
P/O J1
K4
K3
CR1
CR2
C1 10U
PULL TO VOLTAGE RELAY
K1
DATA SWITCH RELAY
K2
A5 W1
GRN
KA
DATA
GND
BLK
A1W3
A1W2
A1W4
TO A2J3
TO A2J2
TO A2J4
C51 330P
FROM DATA PROBE
WHT
PROBE GND
RED


2
3
4
5
6
7
8
9
A1 MAIN ASSEMBLY (05005-60001) SERIES 1928
INTERCONNECTIONS FOR LISTED LINE VOLTAGES
120V
220V
240V
SEE SECTION II FOR INSTRUCTIONS ON PROPER INSERTION OF PC CARD FOR THESE CONNECTIONS)
DAC ADDRESS DECODER
FROM A3J1
FROM A2J1
FAN CONTROL
FAST-BLOW
DAC CURRENT-TO-VOLTAGE TRANSLATORS
TRIGGER THRESHOLD DAC'S
PULL-TO-VOLTAGE GENERATOR
SERVICE/NORM (NORM POSITION)
FEEDBACK SHIFT REGISTER
MAIN DATA PATH
MAIN CLOCK PATH
START/STOP TRACKER FLIP-FLOP
STOP MEASURE FLIP-FLOP
START MEASURE FLIP-FLOP
START/STOP SYNCHRONIZER
STOP/QUAL SYNCHRONIZER
INVERTER
DATA SELECTOR
CLOCK SELECTOR
START/STOP SELECTOR
SELECTOR LOGIC
PROBE-DUAL THRESHOLD → SINGLE THRESHOLD SYNCHRONIZER
DATA PROBE LIGHT DRIVER
EDGE SELECT
MAIN CLOCK
START/STOP
STOP/QUAL
SYNC
STOP/QUAL EDGE
START EDGE
CLOCK EDGE
FROM A3J1 SEE NOTE 4
REGISTER DATA
LSB COUNT
END OF MEASURE
GATE
DATA (PROBE)
TO A3J1
TO A2J1
ANALOG GND
DIGITAL GND
QUAL ENABLE
OUTPUT SHIFT ENABLE
START MEASURE
COUNT
SIGNATURE.T.I
10MHZ
DATA STROBE
COMBINED START/STOP SIGN
FREQ-SIGN
POLARITY DIFF
REAR PANEL CONNECTOR

NOTES:

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN FARADS;
   INDUCTANCE IN HENRIES
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT, AVERAGE VALUE SHOWN.
4. THE FOLLOWING PINS ON CONNECTOR A1J1 APPEAR AT TWO LOCATIONS ON THIS SCHEMATIC.LIKE PIN NUMBERS ARE ELECTICALLY THE SAME POINT: $\overline{19}$, $\overline{20}$, 21, $\overline{21}$, 22, $\overline{23}$, $\overline{24}$, 25, $\overline{25}$, 27

REFERENCE DESIGNATIONS

A1
C1-C32, C34-C51
CR1-CR8
F1
K1-K2
L1-L2
Q1-Q2
R1-R42, R44-R66
S1
U1-U26
VR1-VR3

TABLE OF ACTIVE COMPONENTS

Reference Designation	HP Part Number
CR1, CR2	1901-0033
CR3, CR4	1901-0731
CR5	1906-0069
CR6	1906-0096
CR7	1901-1086
CR8	1902-0522
K1	0490-1219
K2	0490-1220
Q1	1854-0215
Q2	1853-0363
U1, U4, U7, U13	1826-0659
U2	1820-1281
U3	1820-0998
U5	1820-1639
U6	1826-0630
U8, U9, U15, U19	1820-1453
U10, U18, U20	1820-0629
U11, U12	1820-1052
U14	1826-0522
U16	1820-1319
U17	1820-0694
U21	1820-0693
U22	1820-1015
U23	1826-0038
U24	1820-1610
U25	1826-0565
U26	1820-0681
VR1	1826-0221
VR2	1826-0215
VR3	1826-0147

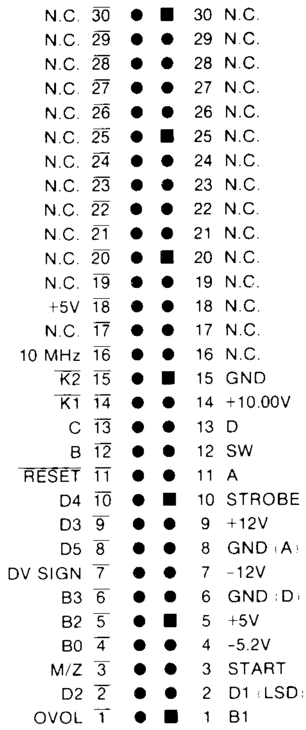
Figure 8-21. A1 Main Assembly/A7 Line Module Schematic Diagram

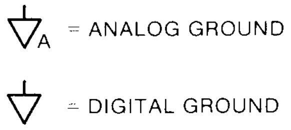
GRID LOCATIONS

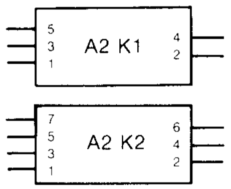
REF DESIG	C/L	SCHEMATIC
A2C1	B-3	C-6
A2C2	B-2	C-7
A2C3	B-4	A-1
A2C4	B-2	B-4
A2C5	C-3	A-3
A2C6	C-3	A-4
A2C7	C-3	A-4
A2C8	C-2	A-5
A2C9	C-3	C-4
A2C10	D-3	A-7
A2C11	D-3	B-7
A2C12	D-4	B-7
A2C13	D-4	C-7
A2C14	D-3	C-4
A2C15	D-3	D-6
A2C16	D-3	E-6
A2C17	D-4	D-5
A2CR1	B-3	A-2
A2CR2	B-3	B-2
A2CR3	B-3	A-2
A2CR4	B-4	C-2
A2CR5	B-4	C-1
A2CR6	C-3	A-2
A2CR7	D-3	B-6
A2K1	B-3	A-2
A2K2	B-3	B-2
A2L1	D-4	D-7
A2L2	D-4	E-7
A2Q1	B-2	B-3
A2Q2	B-2	B-3
A2Q3	B-2	C-3
A2Q4	B-3	C-3
A2Q5	D-4	C-5
A2Q6	D-3	C-7
A2R1	B-2	C-6
A2R2	B-2	C-6
A2R3	B-2	B-6
A2R4	B-4	C-1
A2R5	B-3	B-2
A2R6	B-3	C-3
A2R7	B-3	C-3
A2R8	B-3	A-3
A2R9	B-3	A-3
A2R10	B-3	A-3
A2R11	B-3	C-3
A2R12	B-3	C-3
A2R13	C-3	B-4
A2R14	C-3	A-4
A2R15	C-3	B-4
A2R16	C-3	A-4
A2R17	C-3	A-4
A2R18	C-3	D-3
A2R19	C-3	A-3
A2R20	C-3	D-3
A2R21	C-4	D-3
A2R22	C-4	D-3
A2R23	C-4	D-3
A2R24	C-3	B-3
A2R25	C-3	C-4
A2R26	C-3	C-4
A2R27	C-3	C-4
A2R28	C-3	A-5
A2R29	D-3	C-5
A2R30	D-3	C-5
A2R31	D-3	C-5
A2R32	D-3	B-6
A2R33	D-3	C-6
A2R34	D-3	C-6
A2R35	D-3	D-7
A2R36	D-3	D-4
A2U1	B-3	C-6
A2U2	C-4	D-3
A2U3	C-3	A-3
A2U4	C-2	A-5
A2U5	C-4	D-2
A2U6	D-3	C-5
A2U7	C-2	A-6
A2U8	D-4	E-5
A2U9	D-4	D-5

Part of Figure 8-22. A2 DVM Assembly Schematic Diagram

A2J1 CONNECTOR PINOUT
CIRCUIT SIDE OF BOARD


N.C. $\overline{30}$ 30 N.C.
N.C. $\overline{29}$ 29 N.C.
N.C. $\overline{28}$ 28 N.C.
N.C. $\overline{27}$ 27 N.C.
N.C. $\overline{26}$ 26 N.C.
N.C. $\overline{25}$ 25 N.C.
N.C. $\overline{24}$ 24 N.C.
N.C. $\overline{23}$ 23 N.C.
N.C. $\overline{22}$ 22 N.C.
N.C. $\overline{21}$ 21 N.C.
N.C. $\overline{20}$ 20 N.C.
N.C. $\overline{19}$ 19 N.C.
+5V $\overline{18}$ 18 N.C.
N.C. $\overline{17}$ 17 N.C.
10 MHz $\overline{16}$ 16 N.C.
$\overline{K2}$ $\overline{15}$ 15 GND
$\overline{K1}$ $\overline{14}$ 14 +10.00V
C $\overline{13}$ 13 D
B $\overline{12}$ 12 SW
$\overline{RESET}$ $\overline{11}$ 11 A
D4 $\overline{10}$ 10 STROBE
D3 $\overline{9}$ 9 +12V
D5 $\overline{8}$ 8 GND (A)
DV SIGN $\overline{7}$ 7 -12V
B3 $\overline{6}$ 6 GND (D)
B2 $\overline{5}$ 5 +5V
B0 $\overline{4}$ 4 -5.2V
M/Z $\overline{3}$ 3 START
D2 $\overline{2}$ 2 D1 (LSD)
OVOL $\overline{1}$ 1 B1


A
= ANALOG GROUND
= DIGITAL GROUND


5
3
1
A2 K1
4
2
7
5
3
1
A2 K2
6
4
2

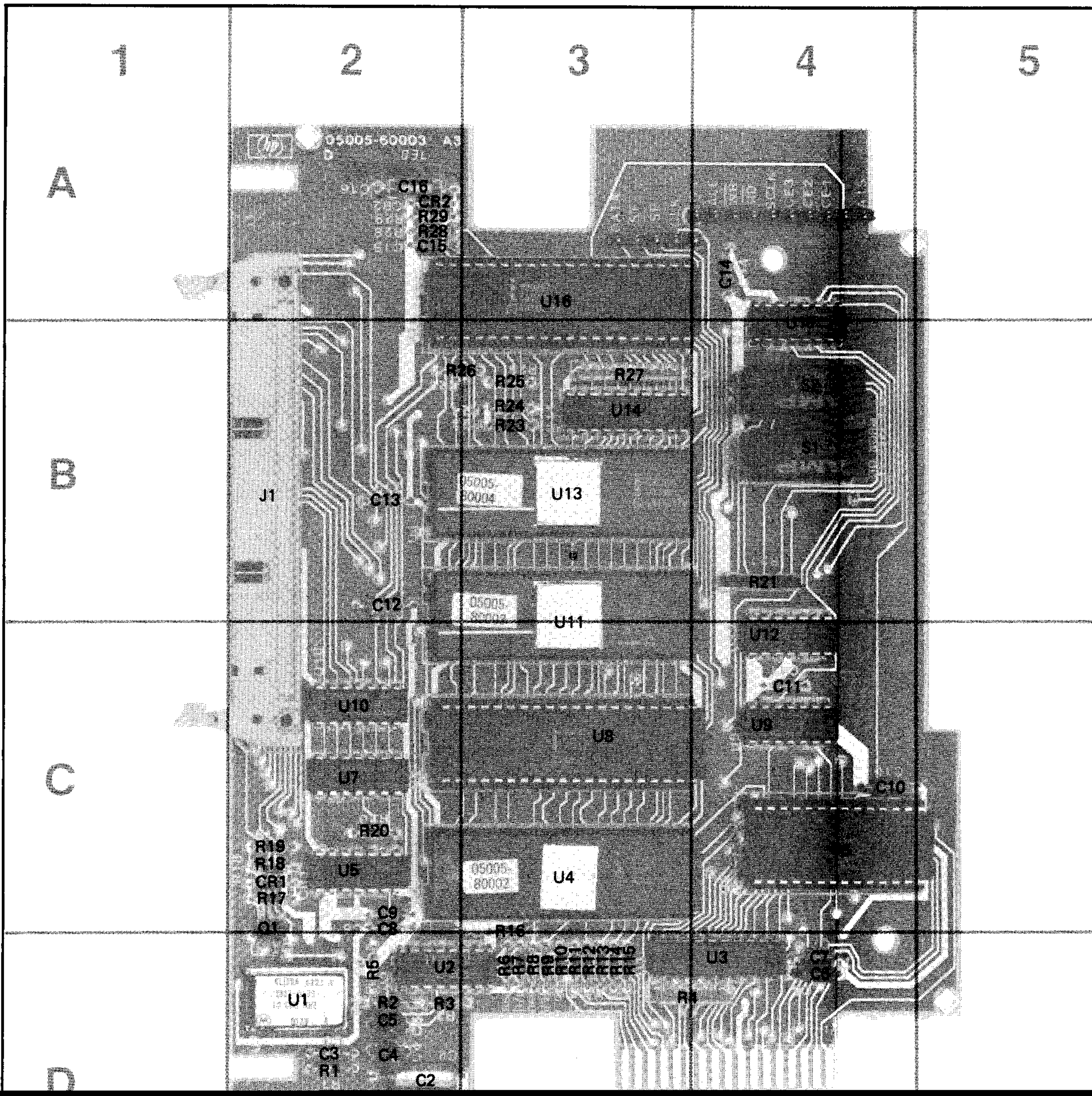
A2 RELAYS PINOUT
TOP VIEW

Troubleshooting:

The following troubleshooting procedures are provided to verify the proper operation, and isolate malfunctioning components on the A2 DVM Assembly. Procedures begin with paragraph 8-264.

Troubleshooting Test	**Diagnostic Number**
Test Point Measurements	—
Zero Offset Value / 25V range	1-0
Zero Offset Value / 250 V range	1-3
Auto-Calibration / 25 V range	1-4
Uncorrected Reading / 25 V range	1-2
Uncorrected Reading / 250 V range	1-5
Zero Offset Value / Ohms Mode	1-6
Reference Voltage / Ohms Mode	1-7
Measured Voltage / Ohms Mode	1-8
Overvoltage Detector Test	—

Part of Figure 8-22. A2 DVM Assembly Schematic Diagram


1
2
3
4
5
A
B
C
D
05005-60003 A3
C16
CR2
R29
R28
C15
U16
C14
U15
R26
R25
R24
R23
R27
U14
S2
S1
J1
C13
05005-80004
U13
05005-80003
U11
C12
R21
U12
C11
U10
U8
U9
U7
C10
R20
R19
R18
CR1
R17
U5
05005-80002
U4
Q1
C9
C8
R16
R6
U2
R5
R7
R8
R9
R10
R11
R12
R13
R14
R15
U3
C7
C6
U1
R2
R3
C5
R4
C3
C4
R1
C2

GRID LOCATIONS

REF DESIG	C/L	SCHEMATIC	REF DESIG	C/L	SCHEMATIC	REF DESIG	C/L	SCHEMATIC
A3C1	E-2	A-1	A3R16	D-3	B-12			
A3C2	E-2	A-1	A3R17	D-2	B-1			
A3C3	D-2	A-1	A3R18	D-2	A-1			
A3C4	D-2	A-11	A3R19	D-2	A-2			
A3C5	D-2	B-11	A3R20	D-2	B-2			
A3C6	D-4	E-13	A3R21	C-4	D-11, E-11			
A3C7	D-4	E-13	A3R22	N/A	N/A			
A3C8	D-2	A-13	A3R23	B-3	B-4			
A3C9	D-2	B-1	A3R24	B-3	B-4			
A3C10	D-4	C-13	A3R25	B-3	E-2			
A3C11	C-4	D-3	A3R26	B-2	B-2			
A3C12	C-2	A-13	A3R27	B-3	A-2, B-2			
A3C13	C-2	C-10	A3R28	B-2	E-3			
A3C14	B-4	C-2	A3R29	B-2	C-3			
A3C15	B-2	A-4						
A3C16	A-2	C-3	A3S1	B-4	D-10			
A3CR1	D-2	A-1	A3S1	B-4	D-10			
A3CR2	B-2	C-3	A3U1	D-2	B-1			
A3Q1	D-2	A-2	A3U2	D-2	B-10			
			A3U3	D-4	E-13			
A3R1	D-2	A-1	A3U4	D-3	B-13			
A3R2	D-2	A-10	A3U5	D-2	B-1			
A3R3	D-2	B-10	A3U6	D-4	C-13			
A3R4	D-2	E-13	A3U7	D-2	D-4, E-6			
A3R5	D-2	A-10	A3U8	C-3	D-5			
A3R6	D-3	B-10	A3U9	C-4	C-11			
A3R7	D-3	B-10	A3U10	C-2	B-2, D-6			
A3R8	D-3	B-11	A3U11	C-3	B-9			
A3R9	D-3	B-13	A3U12	C-4	D-4, E-4			
A3R10	D-3	B-11	A3U13	C-3	D-9			
A3R11	D-3	A-11	A3U14	B-3	D-2			
A3R12	D-3	B-13	A3U15	B-4	C-2			
A3R13	D-3	B-13	A3U16	B-3	C-3			
A3R14	D-3	C-13						
A3R15	D-3	C-13						

Part of Figure 8-23. A3 Microprocessor and Display Drive Assembly Schematic Diagram

Figure 8-22
A2 DVM ASSEMBLY SCHEMATIC DIAGRAM

(See Page 8-99)

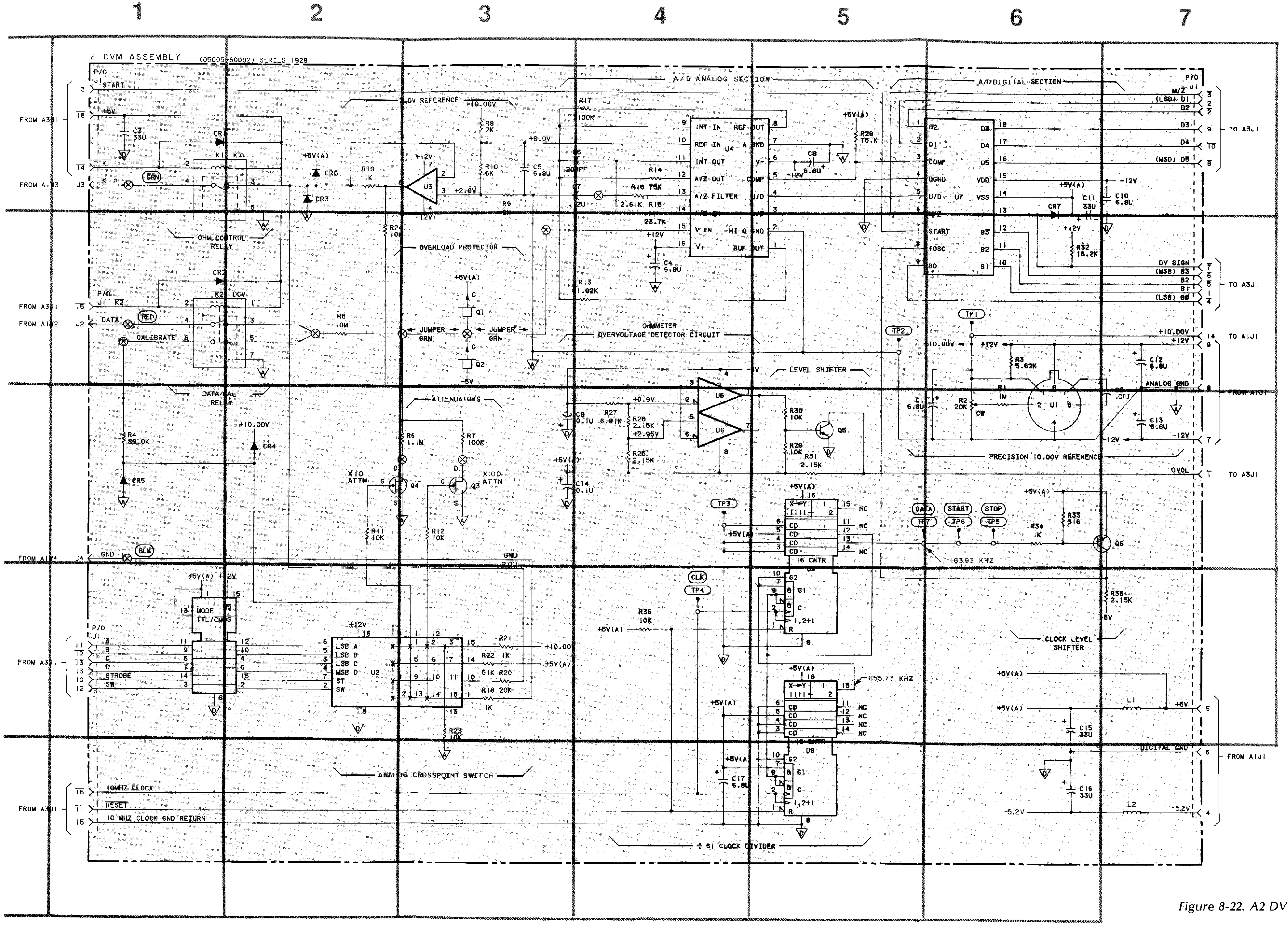

1
2
3
4
5
6
7
2 DVM ASSEMBLY (05005-60002) SERIES 1928
A/D ANALOG SECTION
A/D DIGITAL SECTION
2.0V REFERENCE
OHM CONTROL RELAY
OVERLOAD PROTECTOR
DATA/CAL RELAY
OHMMETER OVERVOLTAGE DETECTOR CIRCUIT
LEVEL SHIFTER
ATTENUATORS
PRECISION 10.00V REFERENCE
ANALOG CROSSPOINT SWITCH
CLOCK LEVEL SHIFTER
÷ 61 CLOCK DIVIDER
FROM A3J1
FROM A1J3
FROM A1J2
FROM A1J4
TO A3J1
TO A1J1
FROM A1J1
START
+5V
K1
K2
DATA
CALIBRATE
GND
10MHZ CLOCK
RESET
10 MHZ CLOCK GND RETURN
STROBE
SW
MODE TTL/CMOS
LSB A
LSB B
LSB C
MSB D
ST
U1
U2
U3
U4
U6
U7
INT IN
REF IN
INT OUT
A/Z OUT
A/Z FILTER
V IN
V+
REF OUT
A GND
COMP
U/D
HI Q GND
BUF OUT
D2
D1
DGND
START
fOSC
B0
D3
D4
D5
VDD
VSS
B3
B2
B1
M/Z
(LSD) D1
(MSD) D5
DV SIGN
(MSB) B3
(LSB) B0
+10.00V
+12V
-12V
ANALOG GND
DIGITAL GND
OVOL
-5.2V
JUMPER GRN
X10 ATTN
X100 ATTN
16 CNTR
U9
U8
163.93 KHZ
655.73 KHZ
TP1
TP2
TP3
TP4
TP5
TP6
TP7
DATA
START
STOP
CLK
GRN
RED
BLK

Figure 8-22. A2 DVM Assembly Schematic Diagram

NOTES:

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN FARADS;
   INDUCTANCE IN HENRIES

REFERENCE DESIGNATIONS

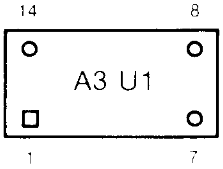
A2
C1-C17 CR1-CR7 K1-K2 L1-L2 Q1-Q6 R1-R36 U1-U9

TABLE OF ACTIVE COMPONENTS

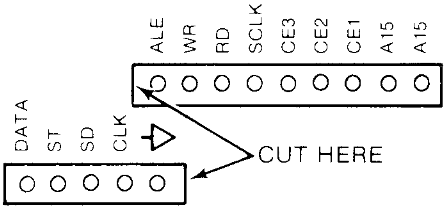
Reference Designation	HP Part Number
CR1, CR2	1901-0731
CR3-CR6	1901-0376
CR7	1901-0033
K1	0490-1219
K2	0490-1220
Q1-Q4	05005-80001
Q5	1854-0215
Q6	1853-0036
U1	1826-0650
U2	1826-0658
U3	1826-0543
U4	1826-0588
U5	1820-2326
U6	1826-0412
U7	1826-0587
U8-U9	1820-1430

A3J1 CONNECTOR PINOUT
CIRCUIT SIDE OF BOARD

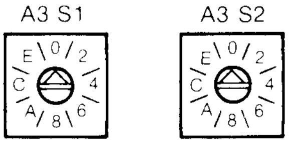
	$\overline{\text{K4}}$	$\overline{30}$	30	END OF MEASURE	
	$\overline{\text{K3}}$	$\overline{29}$	29	LSB COUNT	
	DATA PROBE	$\overline{28}$	28	REGISTER DATA	
	GATE	$\overline{27}$	27	POLARITY DIFF	——TD0
	TD1	$\overline{26}$	26	SYNC	
——TD2	START EDGE	$\overline{25}$	25	CLOCK EDGE	——DA0
——SIGN	$\overline{\text{COMBINED STOP/START}}$	$\overline{24}$	24	$\overline{\text{START MEASURE}}$	
——DA1	STOP/QUAL EDGE	$\overline{23}$	23	$\overline{\text{POP}}$	
	$\overline{\text{OUTPUT SHIFT ENABLE}}$	$\overline{22}$	22	SIGNATURE TI	——TD4
——TD3	DATA STROBE	$\overline{21}$	21	FREQ-SIGN	——$\overline{\text{POP}}$
——TD5	COUNT	$\overline{20}$	20	$\overline{\text{DSTR}}$	
	QUAL ENABLE	$\overline{19}$	19	+5V	——TD7
	+5V	$\overline{18}$	18	+5V	
	GND	$\overline{17}$	17	GND	
	10 MHz	$\overline{16}$	16	GND	
	N.C.	$\overline{15}$	15	GND	
	$\overline{\text{K1}}$	$\overline{14}$	14	N.C.	
	C	$\overline{13}$	13	D	
	B	$\overline{12}$	12	SW	
	N.C.	$\overline{11}$	11	A	
	D4	$\overline{10}$	10	STROBE	
	D3	$\overline{9}$	9	N.C.	
	D5	$\overline{8}$	8	N.C.	
	DV SIGN	$\overline{7}$	7	N.C.	
	B3	$\overline{6}$	6	N.C.	
	B2	$\overline{5}$	5	N.C.	
	B0	$\overline{4}$	4	-5.2V	
	M/Z	$\overline{3}$	3	START	
	D2	$\overline{2}$	2	D1 LSD	
	OVOL	$\overline{1}$	1	B1	



A3 U1 PINOUT TOP VIEW



A3 TEST POINTS TP2-TP16 ARE PROVIDED ON TWO SEPARATE TEST POINT STRIPS. HP PART #1251-4303 IS A 15 TEST POINT STRIP, WHICH IS CUT INTO A 5 TEST POINT AND A 10 TEST POINT STRIP.



TEST SWITCHES A3 S1 AND A3 S2 ARE SIXTEEN POSITION ROTARY SWITCHES, WITH DETENT POSITIONS FOR HEXIDECIMAL CHARACTERS 0 THROUGH F.

Part of Figure 8-23. A3 Microprocessor and Display Drive Assembly Schematic Diagram

A3J2 CONNECTOR PINOUT
CIRCUIT SIDE OF BOARD

34	a
33	b
32	f
31	GATE LIGHT
30	DEVICE ENABLE 2
29	UNCAL
28	UNSTABLE
27	CLOCK EDGE
26	CLOCK EDGE
25	Y2
24	X2
23	Y3
22	DEVICE ENABLE 4
21	Y4
20	X4
19	Y5
18	g
17	c
16	+5V
15	+5V
14	e
13	d
12	ST EDGE
11	ST EDGE
10	X1
9	Y1
8	DEVICE ENABLE 5
7	DEVICE ENABLE 7
6	dp
5	X3
4	DEVICE ENABLE 3
3	DEVICE ENABLE 0
2	DEVICE ENABLE 1
1	DEVICE ENABLE 6

Troubleshooting:

The following troubleshooting procedures are provided to verify the proper operation, and isolate malfunctioning components on the A3 Microprocessor Assembly. Procedures begin with paragraphs 8-256 and 8-267.

Troubleshooting Test	Diagnostic Number
Bus Activity Test	—
ROM Test	0-1
RAM Read Test	0-3
RAM Write Test	0-3
Front Panel Activity Test	—
Freerun ROM Test	2-0
Freerun Address Test	2-0

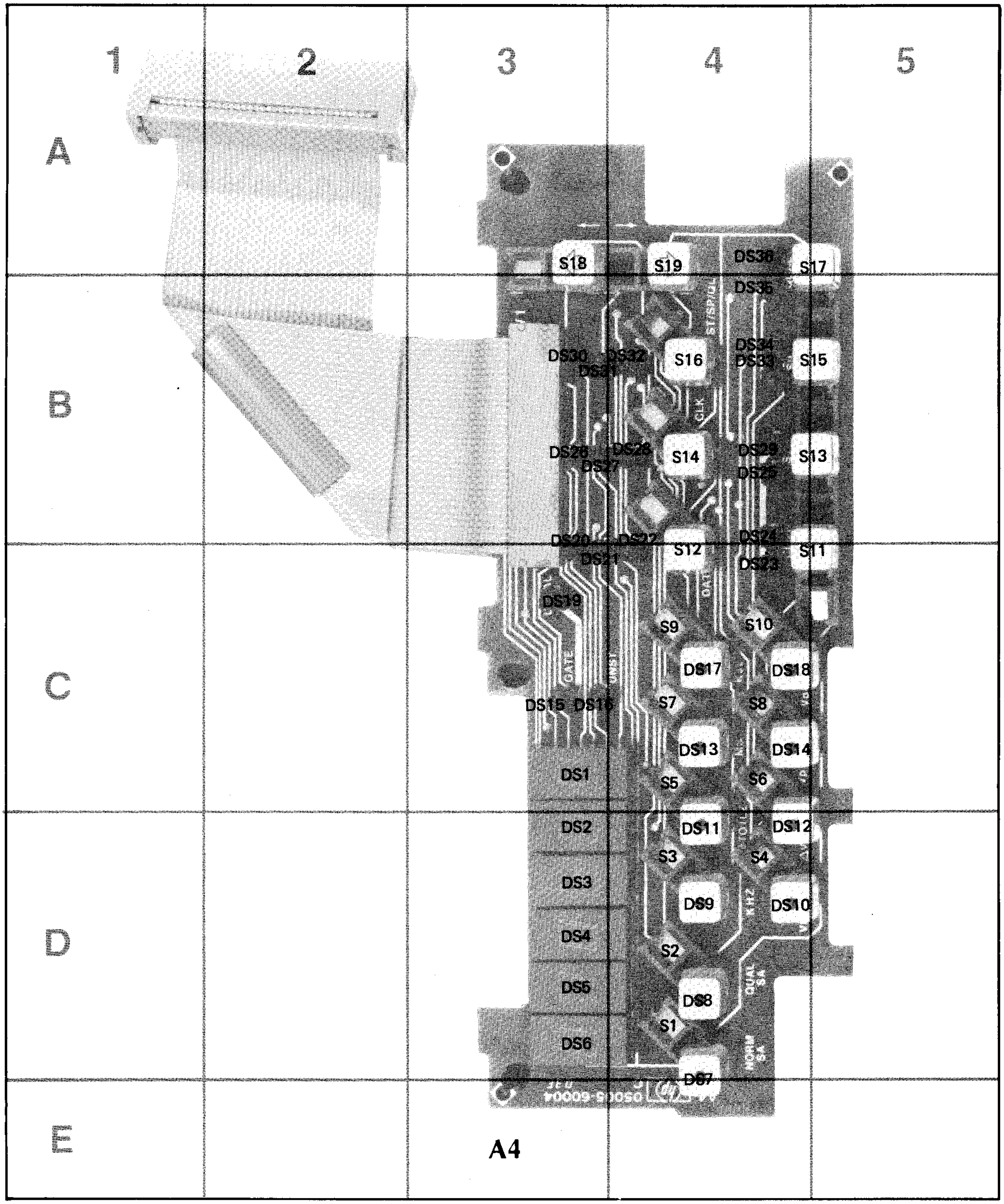
Troubleshooting Test	Diagnostic Number
Output Port Diagnostic	0-4
Timer Diagnostic	0-5

Part of Figure 8-23. A3 Microprocessor and Display Drive Assembly Schematic Diagram

GRID LOCATIONS

REF DESIG	C/L	SCHEMATIC	REF DESIG	C/L	SCHEMATIC	REF DESIG	C/L	SCHEMATIC
A4DS1	D-3	B-7						
A4DS2	D-3	B-6						
A4DS3	D-3	B-5						
A4DS4	D-3	B-4						
A4DS5	D-3	B-3						
A4DS6	E-3	B-2						
A4DS7	E-3	C-2						
A4DS8	D-3	C-3						
A4DS9	D-3	C-2						
A4DS10	D-4	D-2						
A4DS11	D-3	C-2						
A4DS12	D-4	D-2						
A4DS13	D-3	C-3						
A4DS14	D-4	D-3						
A4DS15	C-3	E-3						
A4DS16	C-3	E-2						
A4DS17	C-3	C-3						
A4DS18	C-4	D-3						
A4DS19	C-2	E-2						
A4DS20	C-3	C-5						
A4DS21	C-3	C-5						
A4DS22	C-3	C-5						
A4DS23	C-4	E-5						
A4DS24	C-4	E-4						
A4DS25	B-4	E-4						
A4DS26	B-3	C-4						
A4DS27	B-3	C-3						
A4DS28	B-3	C-4						
A4DS29	B-4	E-3						
A4DS30	B-3	C-4						
A4DS31	B-3	C-5						
A4DS32	B-3	C-4						
A4DS33	B-4	D-4						
A4DS34	B-4	D-4						
A4DS35	B-4	D-5						
A4DS36	B-4	D-5						
A4S1	E-3	C-8						
A4S2	D-3	C-8						
A4S3	D-3	C-6						
A4S4	D-4	C-6						
A4S5	D-3	C-7						
A4S6	D-4	C-7						
A4S7	C-3	C-7						
A4S8	C-4	C-7						
A4S9	C-3	C-6						
A4S10	C-4	C-6						
A4S11	C-4	D-6						
A4S12	C-3	C-6						
A4S13	B-4	D-7						
A4S14	B-3	C-7						
A4S15	B-4	D-7						
A4S16	B-3	C-7						
A4S17	B-4	D-6						
A4S18	B-3	C-8						
A4S19	B-3	C-6						

Part of Figure 8-24. A4 Display and Keyboard Assembly Schematic Diagram

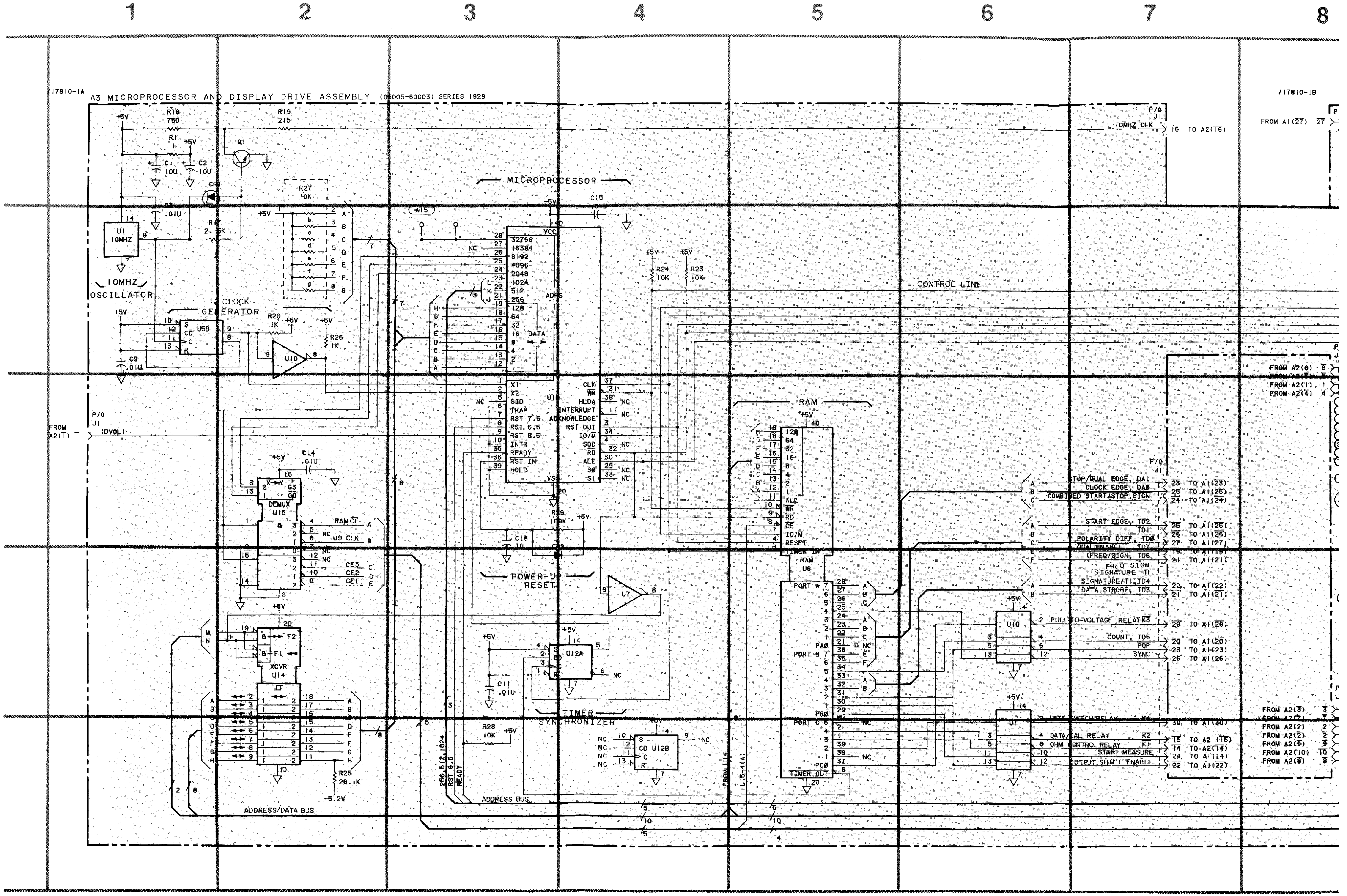

1
2
3
4
5
A
B
C
D
E
S18
S19
DS36
S17
DS35
DS30
DS32
DS31
S16
DS34
DS33
S15
DS26
DS28
DS27
S14
DS29
DS25
S13
DS20
DS22
DS21
S12
DS24
DS23
S11
DS19
S9
S10
DS17
DS18
DS15
DS16
S7
S8
DS13
DS14
DS1
S5
S6
DS2
DS11
DS12
S3
S4
DS3
DS9
DS10
DS4
S2
DS5
DS8
S1
DS6
DS7
05005-60004
QUAL SA
NORM SA
A4

Part of Figure 8-24. A4 Display and Keyboard Assembly Schematic Diagram

Figure 8-23

A3 MICROPROCESSOR AND DISPLAY DRIVE
ASSEMBLY SCHEMATIC DIAGRAM

(See Page 8-101)



717810-1A
A3 MICROPROCESSOR AND DISPLAY DRIVE ASSEMBLY (05005-60003) SERIES 1928
717810-1B
10MHZ OSCILLATOR
U1 10MHZ
÷2 CLOCK GENERATOR
U5B
U10
R18 750
R19 215
R1 1
C1 10U
C2 10U
Q1
CR1
C3 .01U
R17 2.15K
R20 1K
R26 1K
C9 .01U
R27 10K
MICROPROCESSOR
U11
C15 .01U
A15
CONTROL LINE
R24 10K
R23 10K
X1 X2 SID TRAP RST 7.5 RST 6.5 RST 5.5 INTR READY RST IN HOLD
CLK WR HLDA INTERRUPT ACKNOWLEDGE RST OUT IO/M SOD RD ALE SØ S1
ADRS
DATA
FROM A2(T) T
P/O J1 (OVOL)
DEMUX U15
C14 .01U
RAM CE
U9 CLK
CE3 CE2 CE1
XCVR U14
R25 26.1K
-5.2V
ADDRESS/DATA BUS
R29 100K
C16 1U
CR2
POWER-UP RESET
U7
U12A
C11 .01U
TIMER SYNCHRONIZER
R28 10K
U12B
ADDRESS BUS
256,512,1024
RST 6.5
READY
FROM U14
U15-4(A)
RAM
U8
ALE WR RD CE IO/M RESET TIMER IN
PORT A
PORT B
PORT C
PAØ PBØ PCØ
TIMER OUT
10MHZ CLK
TO A2(16)
FROM A1(27)
STOP/QUAL EDGE, DA1
CLOCK EDGE, DAØ
COMBINED START/STOP, SIGN
START EDGE, TD2
TD1
POLARITY DIFF, TDØ
QUAL ENABLE, TD7
(FREQ/SIGN, TD6
FREQ-SIGN SIGNATURE -T1
SIGNATURE/T1, TD4
DATA STROBE, TD3
PULL TO-VOLTAGE RELAY K3
COUNT, TD5
POP
SYNC
DATA SWITCH RELAY K4
DATA/CAL RELAY K2
OHM CONTROL RELAY K1
START MEASURE
OUTPUT SHIFT ENABLE
TO A1(23) TO A1(25) TO A1(24) TO A1(25) TO A1(26) TO A1(27) TO A1(19) TO A1(21) TO A1(22) TO A1(21) TO A1(29) TO A1(20) TO A1(23) TO A1(26) TO A1(30) TO A2(15) TO A2(14) TO A1(14) TO A1(22)
FROM A2(6) FROM A2(1) FROM A2(4)
FROM A2(3) FROM A2(2) FROM A2(9) FROM A2(10) FROM A2(8)

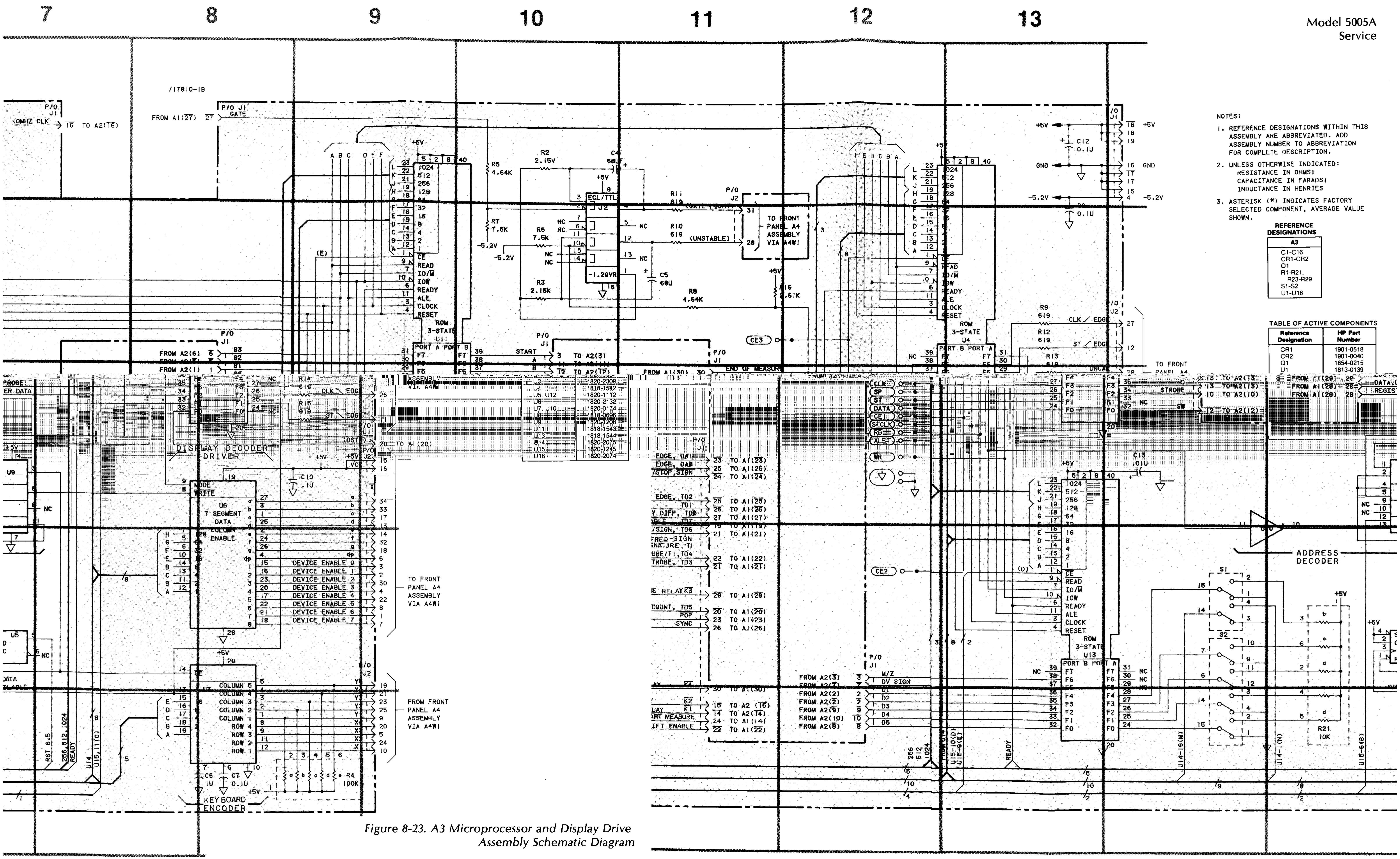

7
8
9
10
11
12
13
/17810-1B
P/O J1
10MHZ CLK
16 TO A2(16)
FROM A1(27) 27
GATE
+5V
1024
512
256
128
64
32
16
8
4
2
1
CE
READ
IO/M
IOW
READY
ALE
CLOCK
RESET
ROM
3-STATE
U11
PORT A
PORT B
R5
4.64K
R7
7.5K
R2
2.15V
C4
68UF
ECL/TTL
U2
R6
7.5K
R3
2.15K
-1.29VR
C5
68U
R8
4.64K
R11
619
(GATE LIGHT)
R10
619
(UNSTABLE)
P/O J2
TO FRONT PANEL A4 ASSEMBLY VIA A4W1
R16
2.61K
CE3
START
TO A2(3)
TO A2(12)
FROM A1(30)
END OF MEASURE
ROM
3-STATE
U4
R9
619
CLK / EDGE
R12
619
ST / EDGE
R13
C12
0.1U
GND
-5.2V
C13
.01U
DISPLAY DECODER DRIVER
U6
7 SEGMENT DATA
COLUMN ENABLE
MODE
WRITE
DEVICE ENABLE 0
DEVICE ENABLE 1
DEVICE ENABLE 2
DEVICE ENABLE 3
DEVICE ENABLE 4
DEVICE ENABLE 5
DEVICE ENABLE 6
DEVICE ENABLE 7
C10
.1U
COLUMN 5
COLUMN 4
COLUMN 3
COLUMN 2
COLUMN 1
ROW 4
ROW 3
ROW 2
ROW 1
FROM FRONT PANEL A4 ASSEMBLY VIA A4W1
C6
1U
C7
0.1U
R4
100K
KEYBOARD ENCODER
U7
U9
U5
RST 6.5
256,512,1024
READY
U14
U15,11(C)
CLK
SP
ST
DATA
CE1
S-CLK
RD
ALE
WR
CE2
EDGE, DA
EDGE, DA0
STOP, SIGN
EDGE, TD2
TD1
DIFF, TD0
SIGN, TD6
FREQ-SIGN
NATURE -T1
URE/T1, TD4
STROBE, TD3
RELAY K3
COUNT, TD5
POP
SYNC
TO A1(23)
TO A1(25)
TO A1(24)
TO A1(25)
TO A1(26)
TO A1(27)
TO A1(19)
TO A1(21)
TO A1(22)
TO A1(21)
TO A1(29)
TO A1(20)
TO A1(23)
TO A1(26)
TO A1(30)
TO A2 (15)
TO A2(14)
TO A1(14)
TO A1(22)
K2
K1
ART MEASURE
IFT ENABLE
FROM A2(3)
FROM A2(7)
FROM A2(2)
FROM A2(2)
FROM A2(9)
FROM A2(10)
FROM A2(8)
M/Z
DV SIGN
D1
D2
D3
D4
D5
ROM
3-STATE
U13
STROBE
SW
TO A2(13)
TO A2(10)
TO A2(12)
FROM A1(29)
FROM A1(28)
DATA
REGIST
U10
ADDRESS DECODER
S1
S2
R21
10K
U14-19(M)
U14-1(N)
U15-6(B)
U15-10(D)
U15-9(E)
FROM U14
NC

Figure 8-23. A3 Microprocessor and Display Drive Assembly Schematic Diagram

NOTES:

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN FARADS;
   INDUCTANCE IN HENRIES
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT, AVERAGE VALUE SHOWN.

REFERENCE DESIGNATIONS

A3
C1-C16 CR1-CR2 Q1 R1-R21, R23-R29 S1-S2 U1-U16

TABLE OF ACTIVE COMPONENTS

Reference Designation	HP Part Number
CR1	1901-0518
CR2	1901-0040
Q1	1854-0215
U1	1813-0139
[illegible]	[illegible]
U3	1820-2309
U4	1818-1542
U5, U12	1820-1112
U6	1820-2132
U7, U10	1820-0174
U8	1818-0696
U9	1820-1208
U11	1818-1543
U13	1818-1544
U14	1820-2075
U15	1820-1245
U16	1820-2074

GRID LOCATIONS

REF DESIG	C/L	SCHEMATIC	REF DESIG	C/L	SCHEMATIC	REF DESIG	C/L	SCHEMATIC
A4DS1	D-3	B-7						
A4DS2	D-3	B-6						
A4DS3	D-3	B-5						
A4DS4	D-3	B-4						
A4DS5	D-3	B-3						
A4DS6	E-3	B-2						
A4DS7	E-3	C-2						
A4DS8	D-3	C-3						
A4DS9	D-3	C-2						
A4DS10	D-4	D-2						
A4DS11	D-3	C-2						
A4DS12	D-4	D-2						
A4DS13	D-3	C-3						
A4DS14	D-4	D-3						
A4DS15	C-3	E-3						
A4DS16	C-3	E-2						
A4DS17	C-3	C-3						
A4DS18	C-4	D-3						
A4DS19	C-2	E-2						
A4DS20	C-3	C-5						
A4DS21	C-3	C-5						
A4DS22	C-3	C-5						
A4DS23	C-4	E-5						
A4DS24	C-4	E-4						
A4DS25	B-4	E-4						
A4DS26	B-3	C-4						
A4DS27	B-3	C-3						
A4DS28	B-3	C-4						
A4DS29	B-4	E-3						
A4DS30	B-3	C-4						
A4DS31	B-3	C-5						
A4DS32	B-3	C-4						
A4DS33	B-4	D-4						
A4DS34	B-4	D-4						
A4DS35	B-4	D-5						
A4DS36	B-4	D-5						
A4S1	E-3	C-8						
A4S2	D-3	C-8						
A4S3	D-3	C-6						
A4S4	D-4	C-6						
A4S5	D-3	C-7						
A4S6	D-4	C-7						
A4S7	C-3	C-7						
A4S8	C-4	C-7						
A4S9	C-3	C-6						
A4S10	C-4	C-6						
A4S11	C-4	D-6						
A4S12	C-3	C-6						
A4S13	B-4	D-7						
A4S14	B-3	C-7						
A4S15	B-4	D-7						
A4S16	B-3	C-7						
A4S17	B-4	D-6						
A4S18	B-3	C-8						
A4S19	B-3	C-6						

Part of Figure 8-24. A4 Display and Keyboard Assembly Schematic Diagram

A4W1 CONNECTOR PINOUT
CIRCUIT SIDE OF BOARD

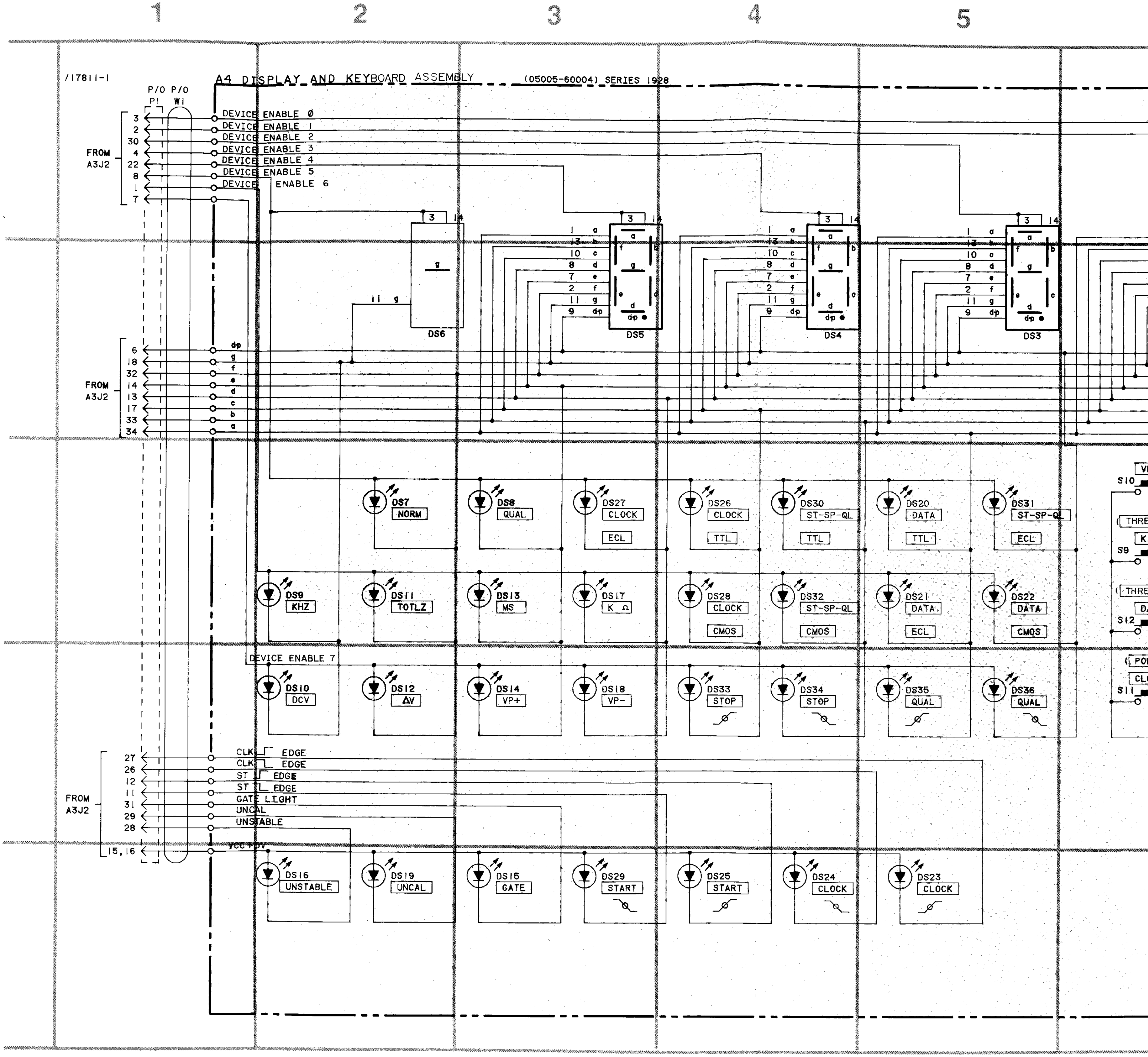
34	a
33	b
32	f
31	GATE LIGHT
30	DEVICE ENABLE 2
29	UNCAL
28	UNSTABLE
27	CLOCK EDGE
26	CLOCK EDGE
25	Y2
24	X2
23	Y3
22	DEVICE ENABLE 4
21	Y4
20	X4
19	Y5
18	g
17	c
16	-5V
15	+5V
14	e
13	d
12	ST EDGE
11	ST EDGE
10	X1
9	Y1
8	DEVICE ENABLE 5
7	DEVICE ENABLE 7
6	dp
5	X3
4	DEVICE ENABLE 3
3	DEVICE ENABLE 0
2	DEVICE ENABLE 1
1	DEVICE ENABLE 6

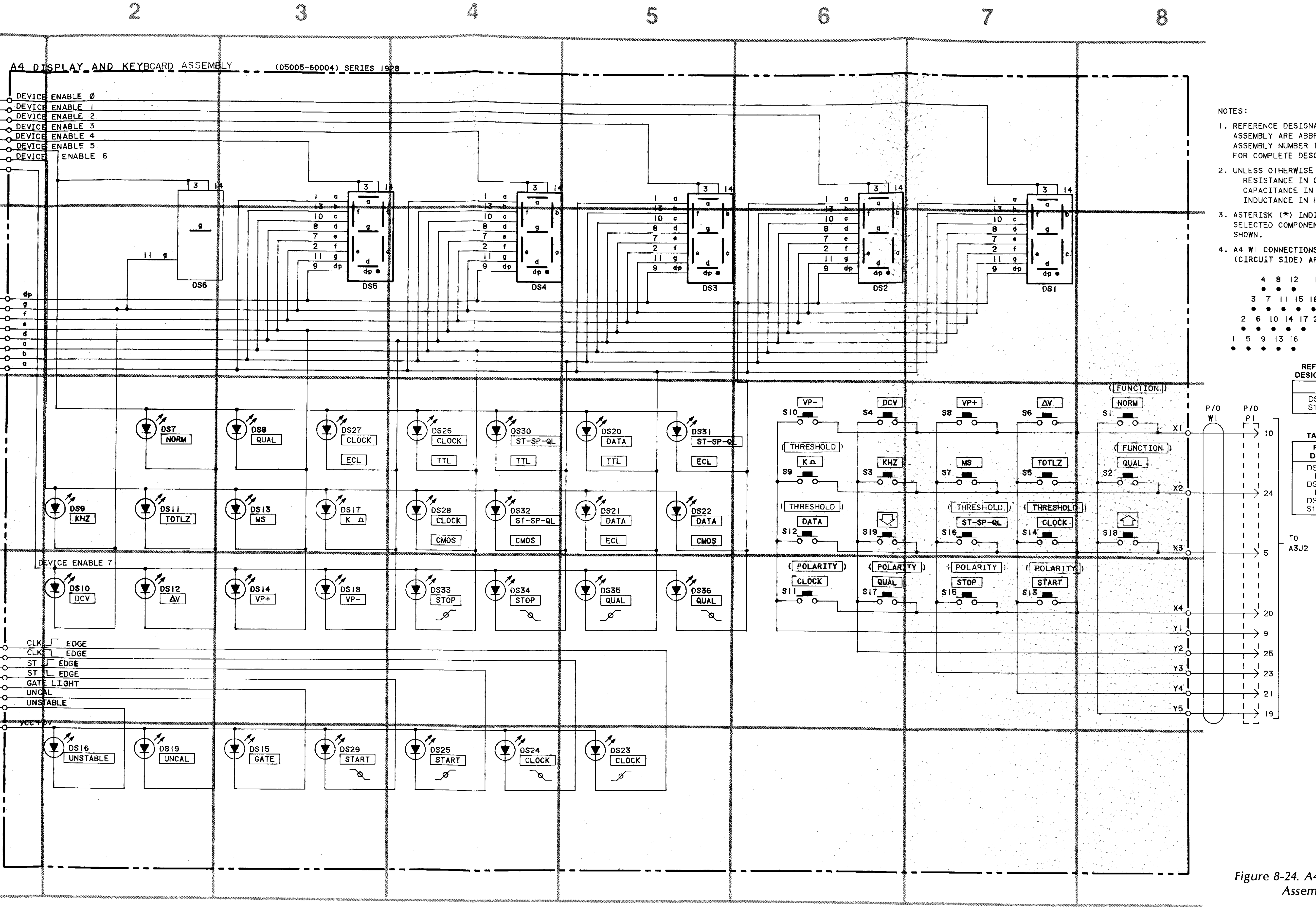
Troubleshooting:

The following troubleshooting procedures are provided to verify the proper operation, and isolate malfunctioning components on the A4 Display Assembly. Procedures begin with paragraph 8-269.

Troubleshooting Test	**Diagnostic Number**
Display Test (Part I)	1-9
Display Test (Part II)	1-A
Keyboard Test	1-B

Part of Figure 8-24. A4 Display and Keyboard Assembly Schematic Diagram


1
2
3
4
5
A
B
C
D
E
/17811-1
A4 DISPLAY AND KEYBOARD ASSEMBLY
(05005-60004) SERIES 1928
P/O P1
P/O W1
FROM A3J2
DEVICE ENABLE 0
DEVICE ENABLE 1
DEVICE ENABLE 2
DEVICE ENABLE 3
DEVICE ENABLE 4
DEVICE ENABLE 5
DEVICE ENABLE 6
DEVICE ENABLE 7
DS6
DS5
DS4
DS3
dp
g
f
e
d
c
b
a
DS7 NORM
DS8 QUAL
DS27 CLOCK ECL
DS26 CLOCK TTL
DS30 ST-SP-QL TTL
DS20 DATA TTL
DS31 ST-SP-QL ECL
DS9 KHZ
DS11 TOTLZ
DS13 MS
DS17 K Ω
DS28 CLOCK CMOS
DS32 ST-SP-QL CMOS
DS21 DATA ECL
DS22 DATA CMOS
DS10 DCV
DS12 ΔV
DS14 VP+
DS18 VP−
DS33 STOP
DS34 STOP
DS35 QUAL
DS36 QUAL
CLK EDGE
CLK EDGE
ST EDGE
ST EDGE
GATE LIGHT
UNCAL
UNSTABLE
VCC +5V
15, 16
DS16 UNSTABLE
DS19 UNCAL
DS15 GATE
DS29 START
DS25 START
DS24 CLOCK
DS23 CLOCK
S10
S9
S12
S11
THRE
K
DA
PO
CL


2
3
4
5
6
7
8
A4 DISPLAY AND KEYBOARD ASSEMBLY
(05005-60004) SERIES 1928
DEVICE ENABLE 0
DEVICE ENABLE 1
DEVICE ENABLE 2
DEVICE ENABLE 3
DEVICE ENABLE 4
DEVICE ENABLE 5
DEVICE ENABLE 6
DEVICE ENABLE 7
dp
g
f
e
d
c
b
a
DS6
DS5
DS4
DS3
DS2
DS1
DS7 NORM
DS8 QUAL
DS27 CLOCK ECL
DS26 CLOCK TTL
DS30 ST-SP-QL TTL
DS20 DATA TTL
DS31 ST-SP-QL ECL
DS9 KHZ
DS11 TOTLZ
DS13 MS
DS17 K Ω
DS28 CLOCK CMOS
DS32 ST-SP-QL CMOS
DS21 DATA ECL
DS22 DATA CMOS
DS10 DCV
DS12 ΔV
DS14 VP+
DS18 VP-
DS33 STOP
DS34 STOP
DS35 QUAL
DS36 QUAL
CLK EDGE
CLK EDGE
ST EDGE
ST EDGE
GATE LIGHT
UNCAL
UNSTABLE
VCC+5V
DS16 UNSTABLE
DS19 UNCAL
DS15 GATE
DS29 START
DS25 START
DS24 CLOCK
DS23 CLOCK
S10 VP-
S4 DCV
S8 VP+
S6 ΔV
S1 (FUNCTION) NORM
(THRESHOLD) KΩ S9
S3 KHZ
S7 MS
S5 TOTLZ
S2 (FUNCTION) QUAL
(THRESHOLD) DATA S12
S19
(THRESHOLD) ST-SP-QL S16
(THRESHOLD) CLOCK S14
S18
(POLARITY) CLOCK S11
(POLARITY) QUAL S17
(POLARITY) STOP S15
(POLARITY) START S13
X1
X2
X3
X4
Y1
Y2
Y3
Y4
Y5
P/O W1
P/O P1
10
24
5
20
9
25
23
21
19
TO A3J2

NOTES:

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN FARADS;
   INDUCTANCE IN HENRIES
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT, AVERAGE VALUE SHOWN.
4. A4 W1 CONNECTIONS TO A4 (CIRCUIT SIDE) ARE AS FOLLOWS:

4 8 12 19 22 26 30 34
● ● ● ● ● ● ● ●
3 7 11 15 18 21 25 29 33
● ● ● ● ● ● ● ● ●
2 6 10 14 17 20 24 28 32
● ● ● ● ● ● ● ● ●
1 5 9 13 16 23 27 31
● ● ● ● ● ● ● ●

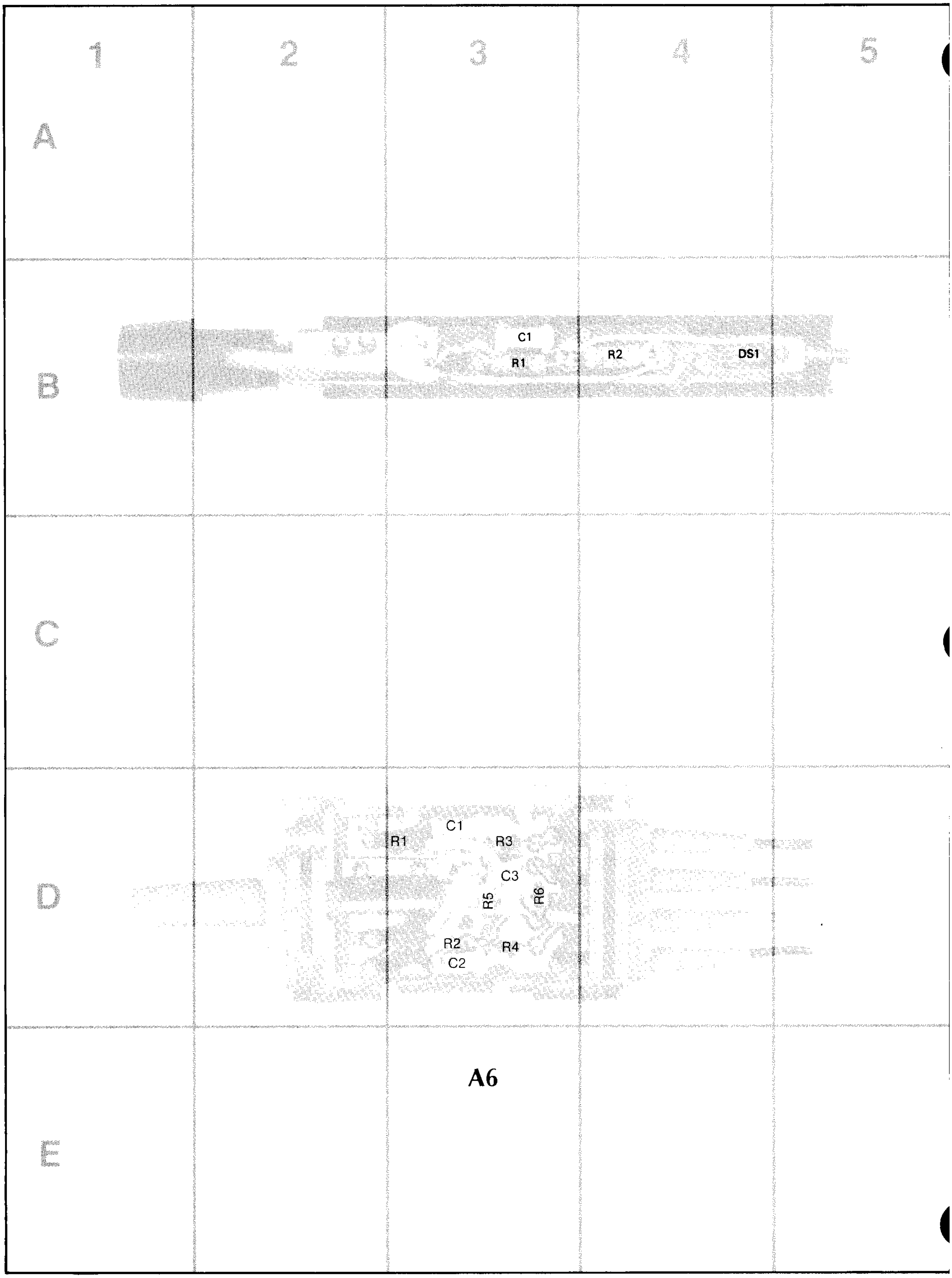
REFERENCE DESIGNATIONS

A4
DS1-DS36 S1-S19

TABLE OF ACTIVE COMPONENTS

Reference Designation	HP Part Number
DS1-DS6	1990-0730
DS7-DS14, DS17, DS18,	1990-0582
DS15, DS16, DS19-DS36	1990-0665
S1-S19	5040-9436

Figure 8-24. A4 Display and Keyboard Assembly Schematic Diagram

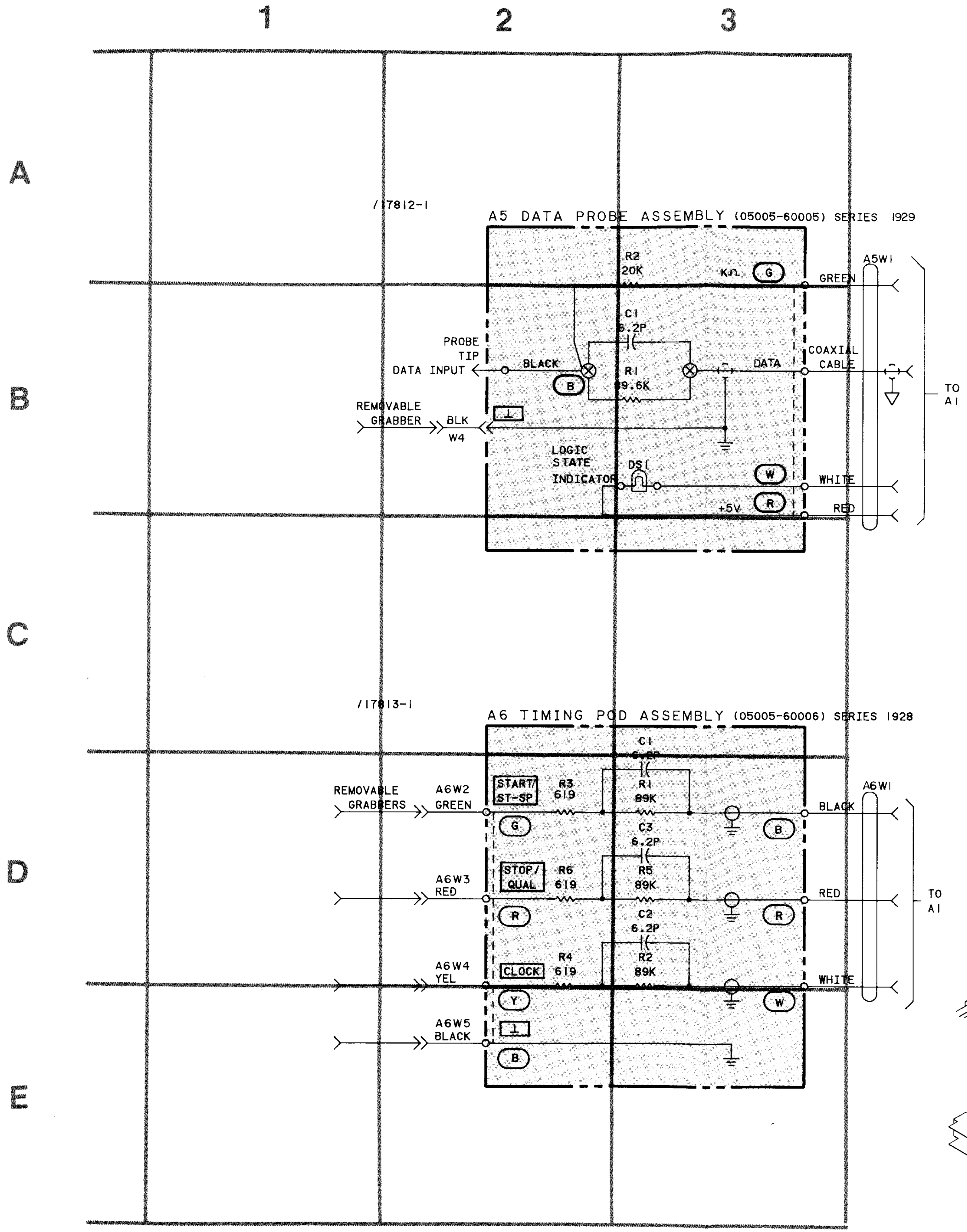

1
2
3
4
5
A
B
C
D
E
C1
R1
R2
DS1
C1
R1
R3
C3
R5
R6
R2
R4
C2
A6

Part of Figure 8-25. A5 Data Probe Assembly/A6 Timing Pod Assembly Schematic Diagram

GRID LOCATIONS

REF DESIG	C/L	SCHEMATIC	REF DESIG	C/L	SCHEMATIC	REF DESIG	C/L	SCHEMATIC
A5C1	B-3	A-2						
A5DS1	B-4	B-2						
A5R1	B-3	B-2						
A5R2	B-3	A-2						
A6C1	D-3	D-2						
A6C2	D-3	D-2						
A6C3	D-3	D-2						
A6R1	D-3	D-2						
A6R2	D-3	E-2						
A6R3	D-3	D-2						
A6R4	D-3	E-2						
A6R5	D-3	D-2						
A6R6	D-4	D-2						

Part of Figure 8-25. A5 Data Probe Assembly/A6 Timing Pod Assembly Schematic Diagram


1
2
3
A
B
C
D
E
/17812-1
A5 DATA PROBE ASSEMBLY (05005-60005) SERIES 1929
R2
20K
KΩ
G
GREEN
A5W1
C1
6.2P
PROBE
TIP
DATA INPUT
BLACK
B
R1
89.6K
DATA
COAXIAL
CABLE
TO
A1
REMOVABLE
GRABBER
BLK
W4
LOGIC
STATE
INDICATOR
DS1
W
WHITE
+5V
R
RED
/17813-1
A6 TIMING POD ASSEMBLY (05005-60006) SERIES 1928
C1
6.2P
REMOVABLE
GRABBERS
A6W2
GREEN
START/
ST-SP
R3
619
R1
89K
A6W1
BLACK
G
B
C3
6.2P
STOP/
QUAL
R6
619
R5
89K
A6W3
RED
RED
R
R
TO
A1
C2
6.2P
A6W4
YEL
CLOCK
R4
619
R2
89K
WHITE
Y
W
A6W5
BLACK
B

NOTES:

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN FARADS;
   INDUCTANCE IN HENRIES
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT, AVERAGE VALUE SHOWN.
4. COAXIAL GROUND IS CONNECTED TO A1 COAXIAL GROUND.

REFERENCE DESIGNATIONS

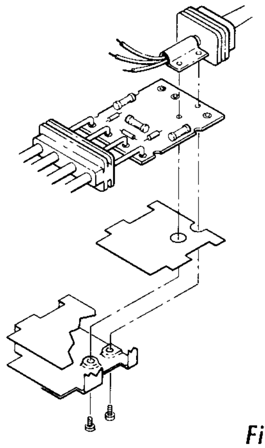
A5
C1 DS1 R1, R2

TABLE OF ACTIVE COMPONENTS

Reference Designation	HP Part Number
DS1	2140-0346

NOTES:

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN FARADS;
   INDUCTANCE IN HENRIES
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT, AVERAGE VALUE SHOWN.
4. THE PLACEMENT OF THE METAL SHIELD WITHIN THE POD IS AS FOLLOWS:



REFERENCE DESIGNATIONS

A6
C1-C3 R1-R6

TABLE OF ACTIVE COMPONENTS

NONE

Figure 8-25. A5 Data Probe Assembly/A6 Timing Pod Assembly Schematic Diagram